



The Carambola3 is a System on Module (SoM) based on the Qualcomm QCA4531 chipset. It is pin-to-pin compatible with the Carambola2 module, meaning that it has the same physical dimensions and pinout as the Carambola2. This allows for easy integration of the Carambola3 into existing systems that use the Carambola2 module. It is a compact and powerful module that integrates a variety of features, including Wi-Fi as well as a range of other interfaces and peripherals. The module is designed for use in a wide range of embedded applications, including Internet of Things (IoT) devices, industrial automation systems, and smart home devices. The QCA4531 chipset provides high performance and low power consumption. The Carambola3 SoM is designed to be easily integrated into a wide range of platforms and products, reducing development time and costs.

### Quick specs

- 802.11b/g/n, 2.4GHz, 150 Mbps data rate, 21 dBm per chain output power;
- U.FI connector or external pin for external antenna;
- 32 MB Flash, 128 MB DDR2 RAM;
- CPU: QCA-4531, 650 MHz clock speed;
- Same pinout and form factor as Carambola2;
- Size: 28 by 38 mm;
- Available interfaces – USB 2.0 host port, 115200 Kbps serial port, 2x 100 Mbps Ethernet, 11x GPIOs;
- Low power consumption, up to 2W.

### Difference between the original Carambola2

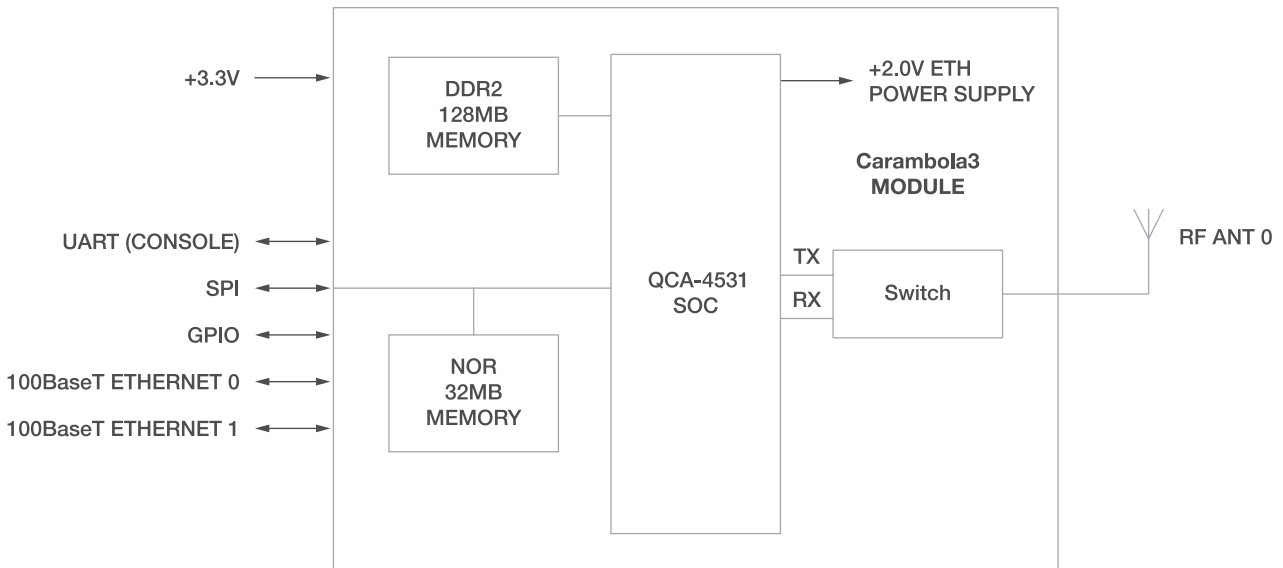
- 250 MHz faster CPU;
- 16 MB larger flash;
- Four GPIO less than Carambola2;
- 64 MB larger RAM.

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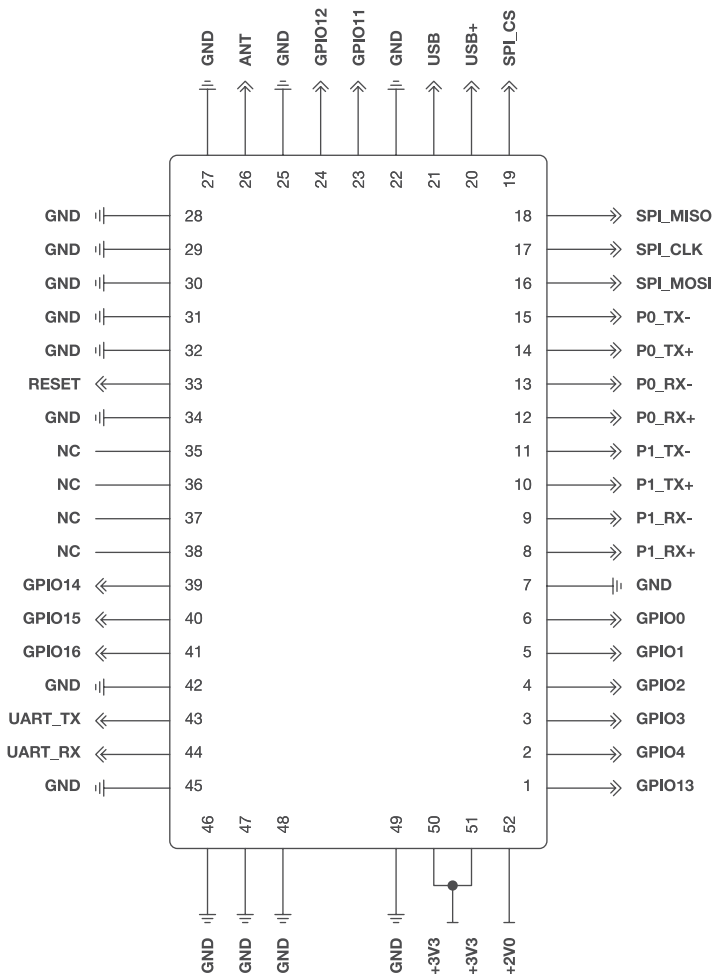
# 1. Block diagram

FIGURE 1-1. BLOCK DIAGRAM



# 2. Module pinout and Pin description

FIGURE 2-1. PIN ASSIGNMENTS



**TABLE 2-1. PINOUT DIFFERENCES BETWEEN CARAMBOLA2 AND CARAMBOLA3**

Pin	Carambola2	Carambola3
1	GPIO23	GPIO13
2	GPIO22	GPIO4
3	GPIO21	GPIO3
4	GPIO20	GPIO2
5	GPIO19	GPIO1
6	GPIO18	GPIO0
16	GPIO4 SPI MOSI	SPI MOSI GPIO7
17	GPIO3 SPI CLK	SPI CLK GPIO6
18	GPIO5 SPI MISO	SPI MISO GPIO8
19	GPIO2 SPI CS0	SPI CS GPIO5
35	LED6 GPIO17	NP
36	LED5 GPIO16	NP
37	LED4 GPIO15	NP
38	LED3 GPIO14	NP
39	LED2 GPIO13	GPIO14
40	LED1 GPIO1	GPIO15
41	LED0 GPIO0	GPIO16

**TABLE 2-2. I/O DESCRIPTION (PAD TYPE) PARAMETERS**

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
RF In/Out	RF input/output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal
Z	High-impedance

**TABLE 2.3. POWER, GROUND AND RESET**

Pin	Pin name	Type	Description
50, 51	VDD33	I	3.3V digital power
52	2.0V	O	2.0V digital power for Ethernet
7, 22, 25, 27, 28, 29, 30, 31, 32, 34, 42, 45, 46, 47, 48, 49	GND	GND	Ground
33	RESET_H	I	Reboot the device

**TABLE 2.4. RADIO**

Pin	Pin name	Type	Description
26	ANT0	RF In/Out	Signal line for antenna

**TABLE 2.5. USB**

Pin	Pin name	Type	Description
20	USB+	IO	USB HS data positive
21	USB-	IO	USB HS data negative

**TABLE 2.6. ETHERNET**

Pin	Pin name	Type	Description
15	P0_TX-	O	ETH0 Transmitter differential signal
14	P0_TX+	O	
13	P0_RX-	I	ETH0 Receiver differential signal
12	P0_RX+	I	
11	P1_TX-	O	ETH1 Transmitter differential signal
10	P1_TX+	O	
9	P1_RX-	I	ETH1 Receiver differential signal
8	P1_RX+	I	

**TABLE 2-7. SPI/UART**

Pin	Pin name	Type	Description
16	SPI_MOSI	O	Data transmission from the Carambola3 to an external device
17	SPI_CLK	O	SPI serial interface clock
18	SPI_MISO	I	Data transmission from an external device to the Carambola3
19	SPI_CS	I/O	SPI chip select
43	UART_RX	I	Serial data in
44	UART_TX		Serial data out
			Bootstrap L: 1: DDR1 0: DDR2

**TABLE 2-8. GPIO**

Pin ID	Pad Name	Voltage	Type	Function	Description
6	GPIO[0]	2.62 V	IO	GPIO_IN_OUT(0)	Configurable I/O
			O	JTAG_TCK	Test Clock
5	GPIO[1]	2.62 V	IO	GPIO_IN_OUT(1)	Configurable I/O
			O	JTAG_TDI	Test Data In
4	GPIO[2]	2.62 V	IO	GPIO_IN_OUT(2)	Configurable I/O
			IO	JTAG_TDO	Test Data Out
3	GPIO[3]	2.62 V	IO	GPIO_IN_OUT(3)	Configurable I/O
			O	JTAG_TMS	Test Mode Select
2	GPIO[4]	2.62 V	IO	GPIO_IN_OUT(4)	Configurable I/O
			I	Bootstrap L	<b>Do not pull up while booting</b>
23	GPIO[11]	2.62 V	IO	GPIO_IN_OUT(11)	Configurable I/O
24	GPIO[12]	2.62 V	IO	GPIO_IN_OUT(12)	Configurable I/O
1	GPIO[13]	2.62 V	IO	GPIO_IN_OUT(13)	Configurable I/O
			O	Bootstrap L	<b>Do not pull up while booting</b>
39	GPIO[14]	2.62 V	IO	GPIO_IN_OUT(14)	Configurable I/O
40	GPIO[15]	2.62 V	IO	GPIO_IN_OUT(15)	Configurable I/O
			I	Bootstrap L	Clock: 0 :25 MHz XTAL (default) 1: 40 MHz XTAL
41	GPIO[16]	2.62 V	IO	GPIO_IN_OUT(16)	Configurable I/O
			I	Bootstrap L	JTAG Mode: 0: JTAG (Default) 1: EJTAG

**NOTE:** Bootstrap pins are for boot configuration, use them cautiously.

### 3. Electrical characteristics

TABLE 3-1. POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage	3.13	3.3	3.46	V
2.0V	Network transformer voltage	1.9	2.0	2.15	V

TABLE 3-2. TEMPERATURE LIMIT RATINGS

Parameter	Minimum	Maximum	Units
Storage Temperature	-65	+150	°C
Commercial Operating Temperature	0	+65	°C
Industrial Operating Temperature	-40	+85	°C
Humidity	10	90	%RH
Storage humidity	5	90	%RH

### 4. Power management

TABLE 4-1. POWER CONSUMPTION

Scenario	Voltage	Current	Total power
TPC duplex throughput and 95% CPU load	5V	0.35A	1.75W
Boot	5V	0.2A	1W
Idle	5V	0.15A	0.95W

### 5. Radio characteristics

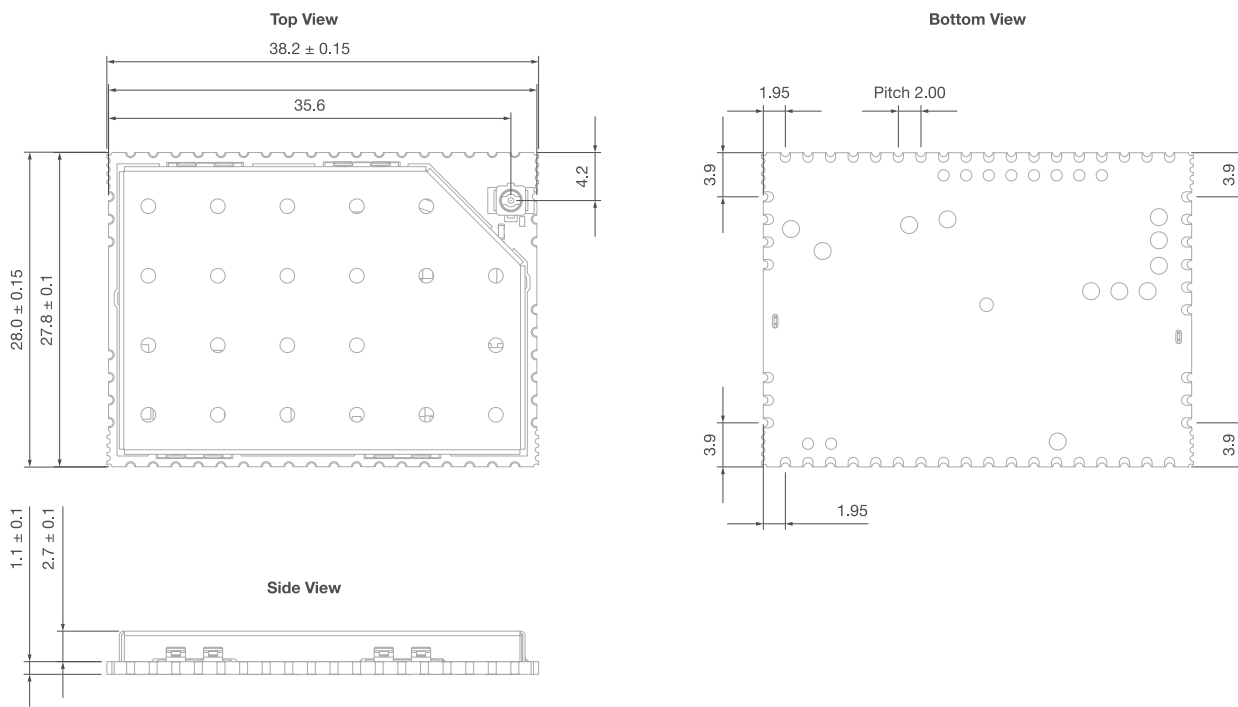
TABLE 5-1. 2.4GHZ 802.11N 20MHZ

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7
Data rate (Mbps)	7.2	14.4	21.7	28.9	43.3	57.8	65	72.2
TX power (dBm)	20	19	19	19	18	17	16	14
RX sensitivity (dB)	-85	-83	-80	-76	-74	-70	-69	-67

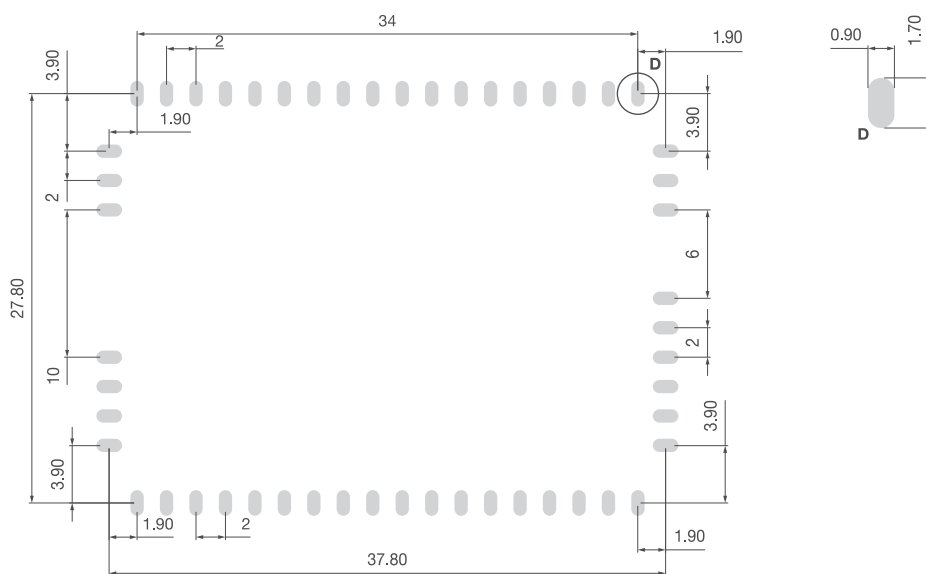
TABLE 5-2. 2.4 GHZ 802.11N 40MHZ

	MCS0	MCS1	MCS2	MCS3	MCS4	MCS5	MCS6	MCS7
Data rate (Mbps)	15	30	45	60	90	120	135	150
TX power (dBm)	20	19	19	19	18	17	16	14
RX sensitivity (dB)	-83	-81	-79	-75	-72	-69	-67	-65

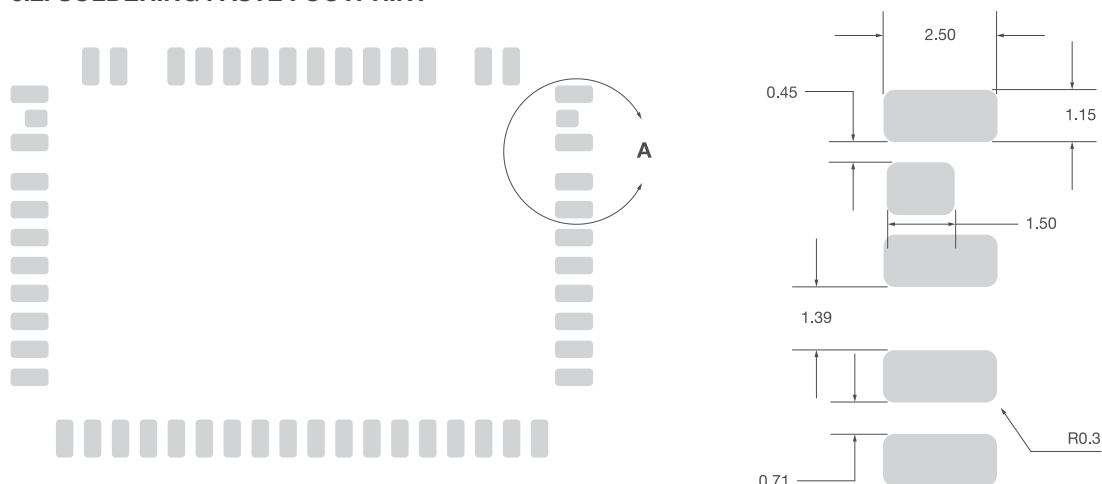
## 6. Mechanical characteristics



### 6.1. PCB FOOTPRINT



### 6.2. SOLDERING PASTE FOOTPRINT



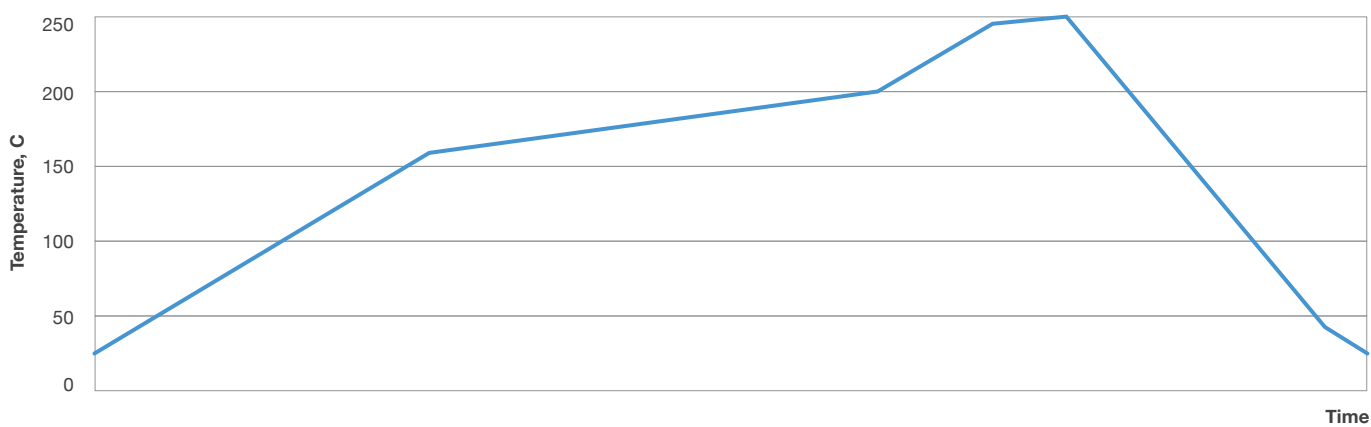


## 7. Reflow profile recommendations

### 7.1 REFLOW PROFILE PARAMETERS

Reflow profile recommendation	
Ramp up rate	3°C/second max
Maximum time maintained above 217°C	120 seconds
Peak temperature	250°C
Maximum time within 5°C of peak temperature	20 seconds
Ramp down rate	6°C/second max

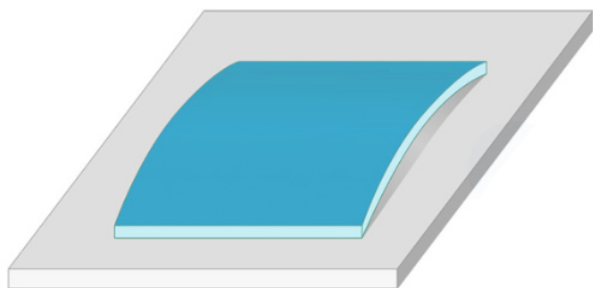
### 7.2 REFLOW PROFILE



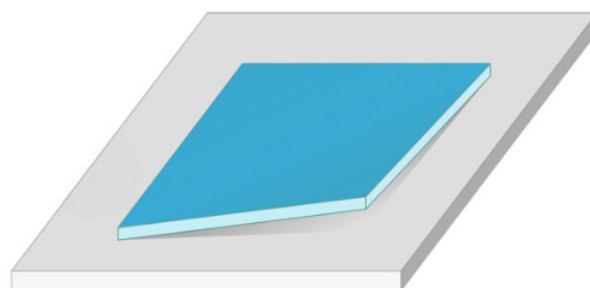
## 8. Laminate Conditions

8devices modules are manufactured according to the standard IPC-A-610 Norm Class 2. Standard states: “Bow/twist after solder should not exceed 1.5% for through-hole and 0.75% for surface mount printed board applications”. According to this statement, Carambola3 module can be bowed and twisted up to 0.285mm. To avoid negative effects of bow and twist we recommend to increase the paste thickness for the module pads to achieve better co-planarity.

**FIGURE 8-1. EXAMPLE OF BOW AND TWIST**

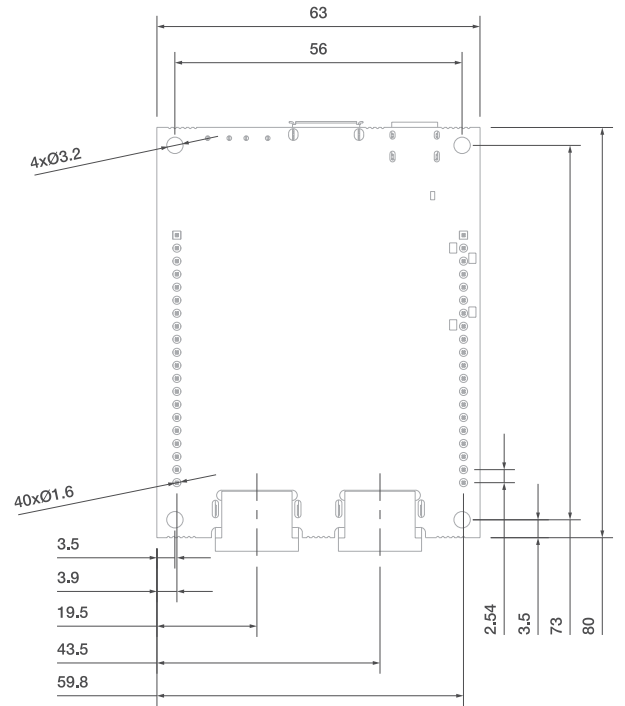
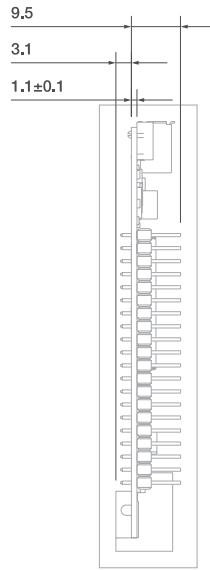
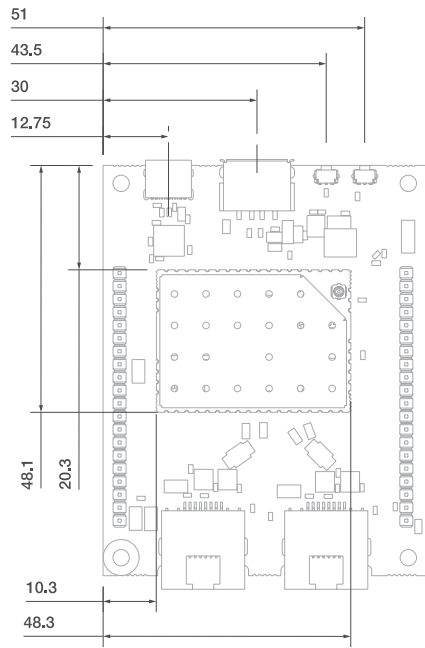


**Bow**



**Twist**

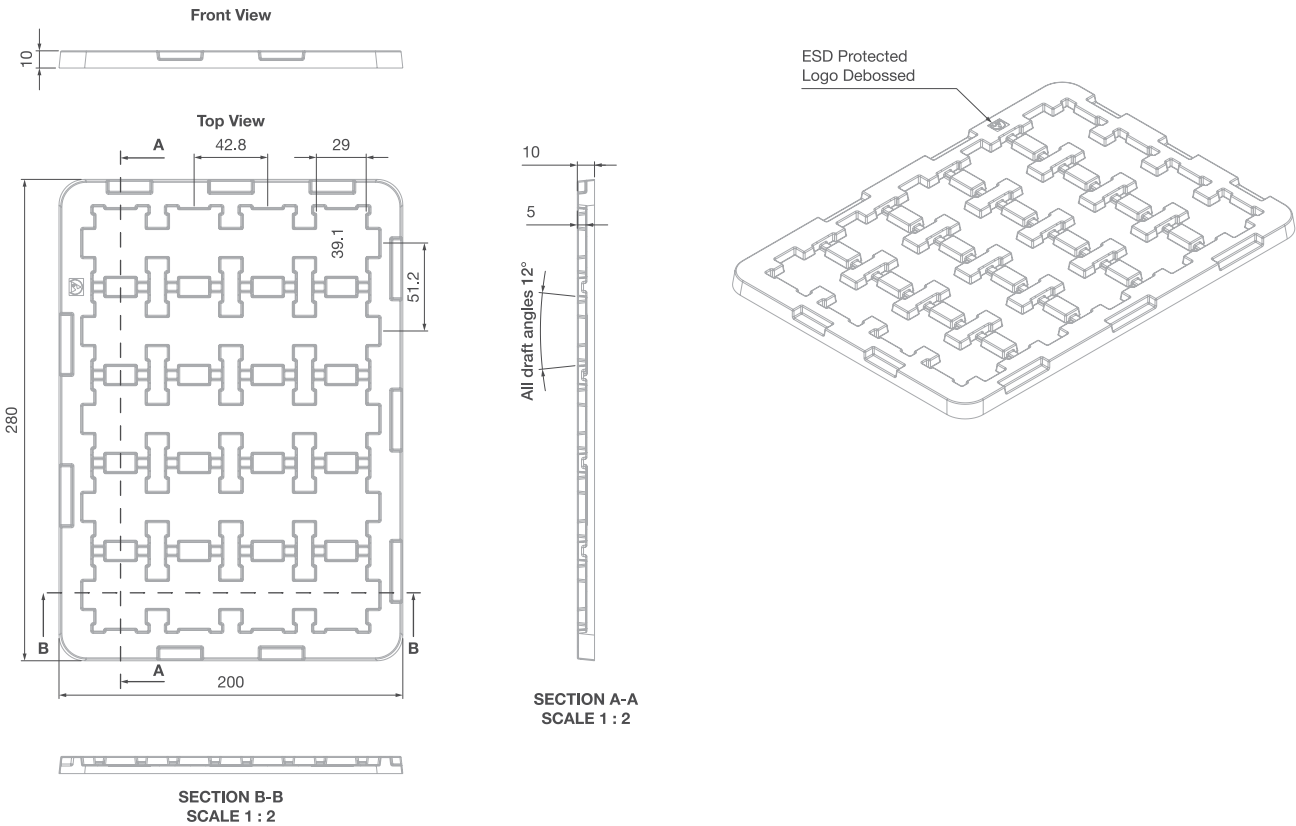
# 9. Development Board



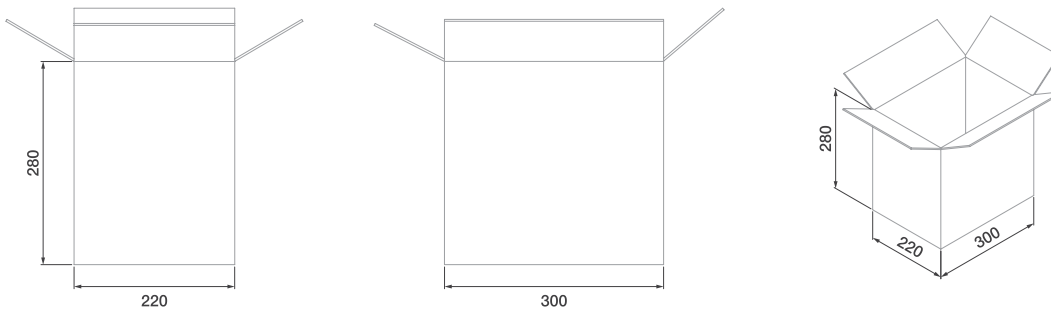
# 10. Carambola3 packaging and ordering info

Carambola3 modules are packed into trays. Each tray fits 20 modules. Every 5 trays are vacuum sealed and one standard packaging box contains 500 modules.

**FIGURE 10-1. CARAMBOLA3 TRAY DIMENSIONS**



**FIGURE 10-2. STANDARD PACKAGING BOX DIMENSIONS**



**TABLE 10-3. ORDERING PART NUMBERS**

Order Number	Description
Carambola3	Carambola3 module, commercial temperature range 0°C to 65°C, QCA-4531 SoC
Carambola3-I	Carambola3 module, industrial temperature range -40°C to 85°C, QCA-4531 SoC
Carambola3 DVK	Development kit, based on Carambola3 module, QCA-4531 SoC

## 11. Document Revision History

Revision	Revision Date	Description
v1.0	2022-11-25	Initial release