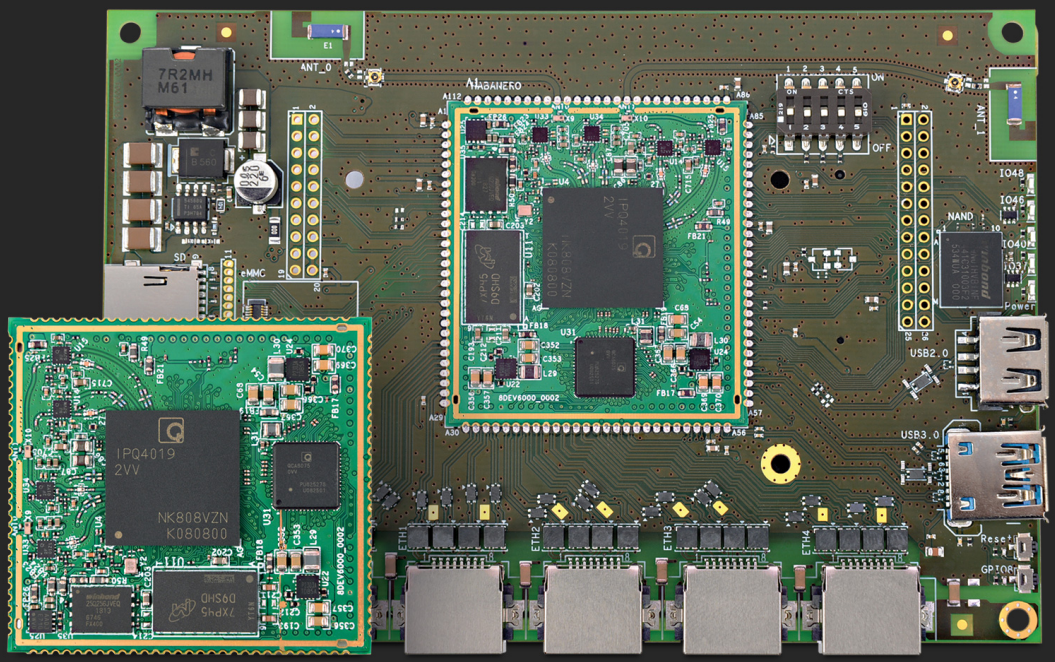


Habanero system on module (SOM) is based on an IPQ4019/IPQ4029 SoC from Qualcomm, which incorporates a powerful quad-core ARM Cortex A7 processor with NEON and FPU. It is ideal for resource demanding applications including routers, gateways and access points. Habanero comes with a high-power, dual-band concurrent radio supporting 802.11ac Wave2 technology (2x2 MiMo). QCA8075C PHY gives support to 5 x Gigabit Ethernet ports. It also has 1 x USB3.0 and 1 x USB2.0 ports and supports other miscellaneous interfaces, which can be configured as general-purpose I/O pins. Hardware based NAT engine and security features like crypto engine, secure boot make it ideal for high-end, fast and secure networking applications. Habanero comes in commercial and industrial temperature versions. Commercial temperature range: 0-65°C, industrial temperature range: -40-85°C.

Quick specs

- Wi-Fi 5 (802.11a/n/ac Wave2) 5GHz with 2x2 MU-MiMo, 866.7Mbps data-rate
- Wi-Fi 5 (802.11b/g/n/ac) 2.4GHz, 400Mbps data-rate
- MIPI DBI v2.0 type B interface
- CPU - IPQ4019/IPQ4029 (716.8MHz)
- OpenWRT Linux flash image
- 24-25 dBm per chain RF output power
- Size - 45 by 49 mm
- Available interfaces – 46 x GPIO, 1 x PCie 2.0, 1 x USB3.0, 1 x USB2.0, 2 x UART, 2 x SPI, 2 x I2C, 4 x PWM, 1 x JTAG, 1 x I2S/TDM, 5 x 1000/100/10 ethernets, 1 x RGMII, 1 x SDIO3.0/eMMC and parallels for NAND flash memory and LCD controller

Table of Contents

1. Features

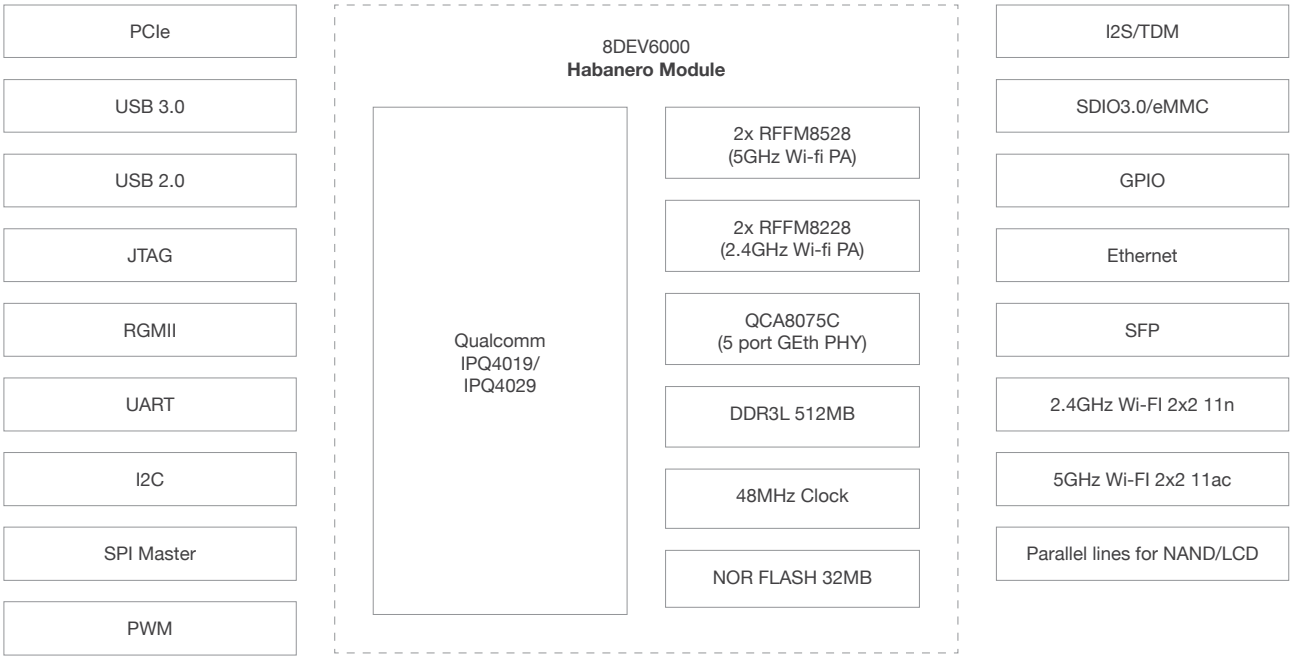
TABLE 1-1. 8DEV6000 HABANERO FEATURES

Feature list			8DEV6000 Habanero
Integrated core	Core type		ARM Cortex-A7 IPQ4019/IPQ4029
	Core clock frequency		716.8MHz
	Cache		256KB L2
Memory	DRAM		DDR3L 512MB (up to 1GB)
	NOR FLASH		32MB
	NAND FLASH (external)		1GB
WIFI	IEEE 802.11 b/g/n/ac 2x2 MU-MIMO 2.4GHz 20/40 MHz 256 QAM		2402-2482MHz 25dBm
	IEEE 802.11 b/g/n/ac 2x2 MU-MIMO 5GHz 20/40/80 MHz 256 QAM		4920-5920MHz 24dBm
RF pin	RF signal is fed to 2 external module pins		2
Display	LCD controller		1
	MIPI DBI v2.0 type B interface (Intel 8080 9bit parallel)		1
Peripherals	PCIe	PCIe 2.0	1
	USB	USB 3.0	1
		USB 2.0	1
	UART	Universal asynchronous receiver transmitter serial ports	2
	SPI	Serial peripheral interface port	2
	I2C	Inter-integrated circuit interfaces for peripheral devices	2
	GPIO	IN/OUT/INT	46
	PWM	Audio Pulse Width Modulation interface	4
	JTAG	Debug interface	1
	I2S/TDM	Multichannel interfaces for digital audio support	1
	Parallel	For parallel NAND flash memory	1
		For parallel LCD controller	1
	Ethernet	Copper 10BASE-Te/100BASE-TX/1000BASE-T	5
		Fiber 100BASE-FX/1000BASE-X	1
	RGMII	Reduced gigabit media independent interface	1
	Reset	Reset button controlled via voltage monitor	1
	SDIO3.0/eMMC	Secure Digital Input Output / Embedded Multi Media Card	1

2. Block diagram

The following figure provides a basic overview of the 8DEV6000 Habanero module.

FIGURE 2-1. 8DEV6000 HABANERO MODULE BLOCK DIAGRAM



3. Module pinout and Pin description

FIGURE 3-1. PIN ASSIGNMENTS

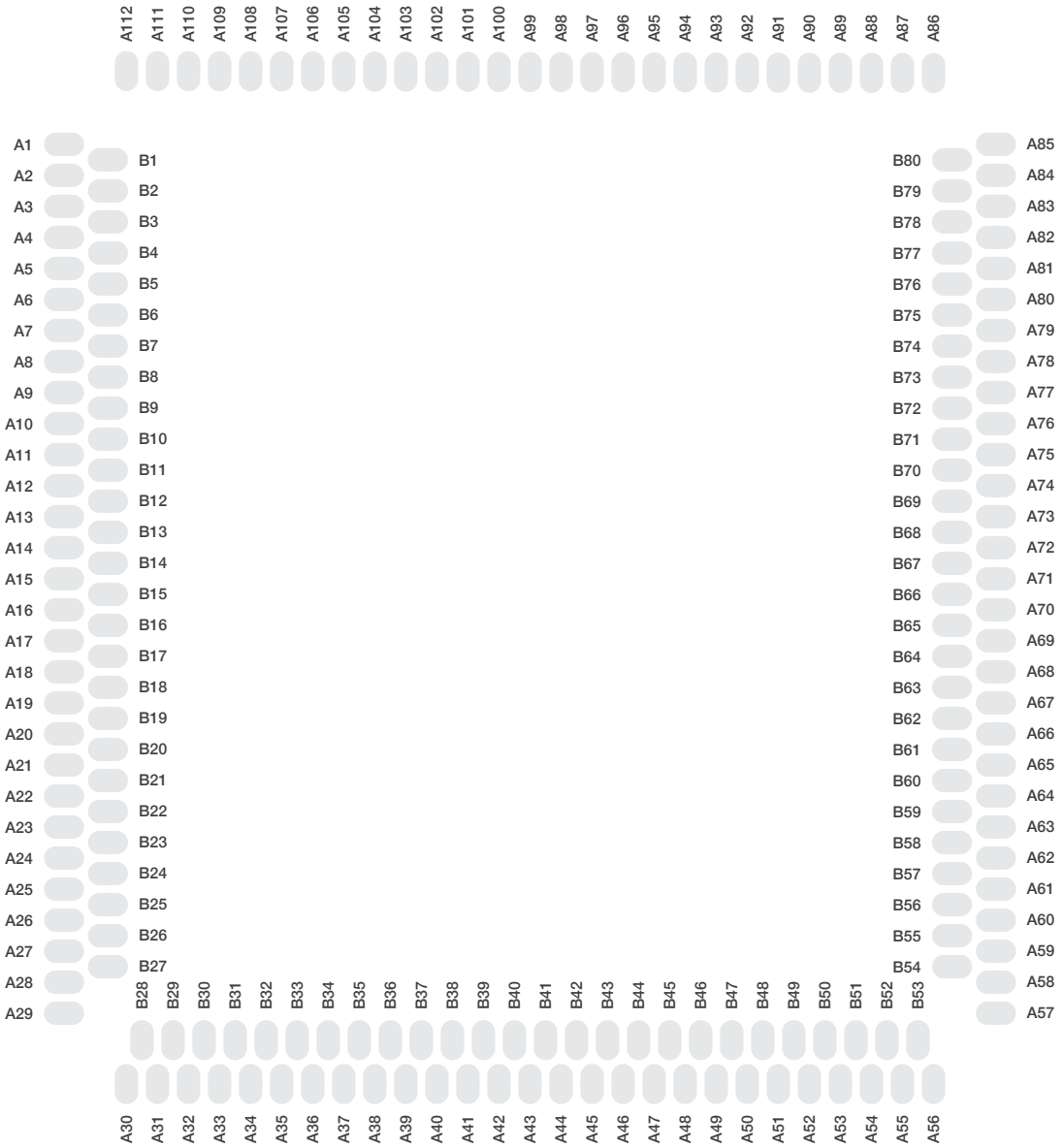


TABLE 3-1. I/O DESCRIPTION (PAD TYPE) PARAMETERS

Symbol	Description
AI	Analog input
AO	Analog output
GND	Ground
RF In/Out	RF input/output
I	Digital input signal
O	Digital output signal
IO	Digital bidirectional signal
OD	Open drain

TABLE 3-2. POWER, GROUND AND RESET

Pin ID	Pin name	Type	Description
A1, A7, A27, A54, A86, B52, B70	DVDD33	I	3.3V digital power
B49	DVDD_2.7V_Malibu	O	2.7V digital power output
A12, A20, A29, A30, A38, A47, A55, A57, A75, A87, A88, A89, A90, A91, A92, A93, A94, A95, A97, A98, A99, A100, A101, A102, A104, A105, A106, A107, A108, A109, A110, A111, A112, B1, B2, B3, B4, B5, B6, B7, B16, B31, B40, B76, B77, B78, B79, B80	GND	GND	Ground
A6	RESET_SOC	I	Reset SoC
B9	CHIP_RST_OUT	I	Reset GEPHY

TABLE 3-3. RADIO

Pin ID	Pin name	Type	Description
A103	TX0	RF In/Out	Signal line for antenna
A96	TX1	RF In/Out	Signal line for antenna

TABLE 3-4. PCIE 2.0

Pin ID	Pin name	Type	Description
B57	PE_CLKN	AO	Clock to PCIe endpoint - negative
A61	PE_CLKP	AO	Clock to PCIe endpoint - positive
B51	PERXN	AI	PCIe receive lane - negative
A53	PERXP	AI	PCIe receive lane - positive
B50	PETXN	AO	PCIe transmit lane - negative
A52	PETXP	AO	PCIe transmit lane - positive

TABLE 3-5. USB 3.0

Pin ID	Pin name	Type	Description
A60	USB1_DP	AI, AO	USB HS data positive
B56	USB1_DM	AI, AO	USB HS data negative
A59	USB1_SS_RX_P	AI	USB SS receive data positive
B55	USB1_SS_RX_N	AI	USB SS receive data negative
B53	USB1_SS_TX_P	AO	USB SS transmit data positive
A56	USB1_SS_TX_N	AO	USB SS transmit data negative

TABLE 3-6. USB 2.0

Pin ID	Pin name	Type	Description
B54	USB2_DP	AI, AO	USB HS data positive
A58	USB2_DM	AI, AO	USB HS data negative

TABLE 3-7. GIGABIT ETHERNET

Pin ID	Pin name	Type	Description
B23	P0_TRX0-	AI, AO	PHY0 MDI pair0 negative, connect to transformer
A23	P0_TRX0+	AI, AO	PHY0 MDI pair0 positive, connect to transformer
B24	P0_TRX1-	AI, AO	PHY0 MDI pair1 negative, connect to transformer
A24	P0_TRX1+	AI, AO	PHY0 MDI pair1 positive, connect to transformer
B25	P0_TRX2-	AI, AO	PHY0 MDI pair2 negative, connect to transformer
A25	P0_TRX2+	AI, AO	PHY0 MDI pair2 positive, connect to transformer
B26	P0_TRX3-	AI, AO	PHY0 MDI pair3 negative, connect to transformer
A26	P0_TRX3+	AI, AO	PHY0 MDI pair3 positive, connect to transformer
A28	P1_TRX0-	AI, AO	PHY1 MDI pair0 negative, connect to transformer
B27	P1_TRX0+	AI, AO	PHY1 MDI pair0 positive, connect to transformer
A31	P1_TRX1-	AI, AO	PHY1 MDI pair1 negative, connect to transformer
B28	P1_TRX1+	AI, AO	PHY1 MDI pair1 positive, connect to transformer
A32	P1_TRX2-	AI, AO	PHY1 MDI pair2 negative, connect to transformer
B29	P1_TRX2+	AI, AO	PHY1 MDI pair2 positive, connect to transformer
A33	P1_TRX3-	AI, AO	PHY1 MDI pair3 negative, connect to transformer
B30	P1_TRX3+	AI, AO	PHY1 MDI pair3 positive, connect to transformer
B32	P2_TRX0-	AI, AO	PHY2 MDI pair0 negative, connect to transformer
A34	P2_TRX0+	AI, AO	PHY2 MDI pair0 positive, connect to transformer
B33	P2_TRX1-	AI, AO	PHY2 MDI pair1 negative, connect to transformer
A35	P2_TRX1+	AI, AO	PHY2 MDI pair1 positive, connect to transformer
B34	P2_TRX2-	AI, AO	PHY2 MDI pair2 negative, connect to transformer

Pin ID	Pin name	Type	Description
A36	P2_TRX2+	AI, AO	PHY2 MDI pair2 positive, connect to transformer
B35	P2_TRX3-	AI, AO	PHY2 MDI pair3 negative, connect to transformer
A37	P2_TRX3+	AI, AO	PHY2 MDI pair3 positive, connect to transformer
A39	P3_TRX0-	AI, AO	PHY3 MDI pair0 negative, connect to transformer
B36	P3_TRX0+	AI, AO	PHY3 MDI pair0 positive, connect to transformer
A40	P3_TRX1-	AI, AO	PHY3 MDI pair1 negative, connect to transformer
B37	P3_TRX1+	AI, AO	PHY3 MDI pair1 positive, connect to transformer
A41	P3_TRX2-	AI, AO	PHY3 MDI pair2 negative, connect to transformer
B38	P3_TRX2+	AI, AO	PHY3 MDI pair2 positive, connect to transformer
A42	P3_TRX3-	AI, AO	PHY3 MDI pair3 negative, connect to transformer
B39	P3_TRX3+	AI, AO	PHY3 MDI pair3 positive, connect to transformer
B41	P4_TRX0-	AI, AO	PHY4 MDI pair0 negative, connect to transformer
A43	P4_TRX0+	AI, AO	PHY4 MDI pair0 positive, connect to transformer
B42	P4_TRX1-	AI, AO	PHY4 MDI pair1 negative, connect to transformer
A44	P4_TRX1+	AI, AO	PHY4 MDI pair1 positive, connect to transformer
B43	P4_TRX2-	AI, AO	PHY4 MDI pair2 negative, connect to transformer
A45	P4_TRX2+	AI, AO	PHY4 MDI pair2 positive, connect to transformer
B44	P4_TRX3-	AI, AO	PHY4 MDI pair3 negative, connect to transformer
A46	P4_TRX3+	AI, AO	PHY4 MDI pair3 positive, connect to transformer
A48	SFP_SOP	AO	1.25 Gbps differential data positive output for SGMII or 1000BASE-X
B45	SFP_SON	AO	1.25 Gbps differential data negative output for SGMII or 1000BASE-X
A49	SFP_SIP	AI	1.25 Gbps differential data positive input for SGMII or 1000BASE-X
B46	SFP_SIN	AI	1.25 Gbps differential data negative input for SGMII or 1000BASE-X
B20	P0_100_LED	O	LED output for 100BASE-TX or 10BASE-Te of PHY0
B21	P0_1000_LED	O	LED output for 1000BASE-T of PHY0
A21	P1_100_LED	O	LED output for 100BASE-TX or 10BASE-Te of PHY1
B22	P1_1000_LED	O	LED output for 1000BASE-T of PHY1
B19	P2_100_LED	O	LED output for 100BASE-TX or 10BASE-Te of PHY2
A22	P2_1000_LED	O	LED output for 1000BASE-T of PHY2
A50	P3_100_LED	O	LED output for 100BASE-TX or 10BASE-Te of PHY3
B47	P3_1000_LED	O	LED output for 1000BASE-T of PHY3
A51	P4_100_LED	O	LED output for 100BASE-TX or 10BASE-Te of PHY4
B48	P4_1000_LED	O	LED output for 1000BASE-T of PHY4

TABLE 3-8. NAND/LCD CONTROLLER

Pin ID	Pin name	Type	Description
B67	QPIC_PAD_DAT0	O	NAND/LCD controller data
A73	QPIC_PAD_DAT1	O	NAND/LCD controller data
A76	QPIC_PAD_DAT2	O	NAND/LCD controller data
B71	QPIC_PAD_DAT3	O	NAND/LCD controller data
A69	QPIC_PAD_DAT4	O	NAND/LCD controller data
B66	QPIC_PAD_DAT5	O	NAND/LCD controller data
A72	QPIC_PAD_DAT6	O	NAND/LCD controller data
B65	QPIC_PAD_DAT7	O	NAND/LCD controller data
B75	QPIC_PAD_DAT8	O	NAND/LCD controller data
A66	NAND_BUSY_N	I, OD	NAND controller busy_not_ready input. Active low
A67	NAND_WE_N	O	NAND/LCD controller write enable
B63	NAND_OE_N	O	NAND/LCD controller read enable
A70	NAND_CLE_N	O	NAND controller CLE/LCD controller DCX. CLE is command latch enable. Active high. DCX is data/command. 1 is data, o is command
A68	NAND_CS_N	O	NAND controller chip select
B64	NAND_ALE_N	O	NAND controller ALE. Active high

TABLE 3-9. GPIO

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
A84	GPIO0	0	GPIO	3.3		
		1	JTAG TDI[1]	3.3	I	JTAG test data in
A83	GPIO1	0	GPIO	3.3		
		1	JTAG TCK[1]	3.3	I	JTAG test clock
A85	GPIO2	0	GPIO	3.3		
		1	JTAG TMS[1]	3.3	IO	JTAG test mode state
A81	GPIO3	0	GPIO	3.3		
		1	JTAG TDO[1]	3.3	O	JTAG test data out
			BOOT_CONFIG(0)	3.3	I	
A82	GPIO4	0	GPIO	3.3		
		1	JTAG RST_N[1]	3.3	I	JTAG reset for debug
A80	GPIO5	0	GPIO	3.3		
		1	JTAG TRST_N[1]	3.3	I	JTAG test reset
A2	GPIO8	0	GPIO	3.3		
		1	BLSP_UART1_TXD		O	Tx data
		2	WIFI0_UART_TXD		O	Wi-Fi UART output
		3	WIFI1_UART_TXD		O	Wi-Fi UART output

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
A5	GPIO9	0	GPIO	3.3		
		1	BLSP_UART1_RXD		I	Rx data
		2	WIFI0_UART_RXD(0)		I	Wi-Fi UART input
		3	WIFI1_UART_RXD(0)		I	Wi-Fi UART input
		5	WIFI0_UART_TXD		O	Wi-Fi UART output
A4	GPIO10	0	GPIO	3.3		
		1	BLSP_UART1_CTS		I	Clear to send
		2	WIFI0_UART_CTS(0)		I	Wi-Fi UART input
		3	WIFI1_UART_CTS(0)		I	Wi-Fi UART input
		4	BLSP_I2C0_SCK(0)		I/O, OD	I²C0 SCK
A3	GPIO11	0	GPIO	3.3		
		1	BLSP_UART1_RTS		O	Ready to send
		2	WIFI0_UART_RTS		O	Wi-Fi UART output
		3	WIFI1_UART_RTS		O	Wi-Fi UART output
		4	BLSP_I2C0_SDA(0)		I/O, OD	I²C0 SDA
A10	GPIO14	0	GPIO	3.3		
		1	BLSP_SPI0_MOSI(0)		O	SPI0 Master-out Slave-in data
A8	GPIO16	0	GPIO	3.3		
		1	BLSP_UART0_RXD		I	Rx data
		2	LED(0)			Led_clk or led_dar or led_strobe
B8	GPIO17	0	GPIO	3.3		
		1	BLSP_UART0_TXD		O	
		2	LED(1)			UART output
A9	GPIO18	0	GPIO	3.3		
		1	WIFI0_UART_CTS(1)		I	Wi-Fi UART input
		2	WIFI1_UART_CTS(1)		I	Wi-Fi UART input
B10	GPIO20	0	GPIO	3.3		
		1	BLSP_I2C0_SCK(1)		I/O, OD	I²C0 SCK
		2	AUDIO_RXMCLK(0)	3.0	I/O	Master clock source of Audio I²S/ TDM Rx interface
A11	GPIO21	0	GPIO	3.3		
		1	BLSP_I2C0_SDA(1)		I/O, OD	I²C0 SDA
		2	AUDIO_RXBCLK(1)	3.0	I/O	Bit clock of Audio I²S/TDM Rx interface
B11	GPIO22	0	GPIO	3.3		
		1	RGMII_RXD(0)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 0
		2	AUDIO_RXFSYNC(1)	3.0	I/O	Left or Right indication of Audio I²S Rx interface and frame start indication of Audio TDM Rx interface

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
A13	GPIO23	0	GPIO	3.3		
		1	SDIO_DAT(0)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 0
		2	RGMII_RXD(1)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 1
		3	AUDIO_RXD(1)	3.0	I	Serial digital data of Audio Rx interface
B12	GPIO24	0	GPIO	3.3		
		1	SDIO_DAT(1)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 1
		2	RGMII_RXD(2)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 2
		3	AUDIO_TXMCLK(0)	3.0	I/O	Master clock source of Audio I²S/ TDM Tx interface
A14	GPIO25	0	GPIO	3.3		
		1	SDIO_DAT(2)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 2
		2	RGMII_RXD(3)	1.5(2.0)/2.5(1.0)	I	RGMII Data input 3
		3	AUDIO_TXBCLK(0)	3.0	I/O	Bit clock of Audio I²S/TDM Tx interface
B13	GPIO26	0	GPIO	3.3		
		1	SDIO_DAT(3)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 3
		2	RGMII_RX_CTL	1.5(2.0)/2.5(1.0)	I	RGMII Rx control
		3	AUDIO_TXFSYNC(0)	3.0	I/O	Left or Right indication of Audio I²S Tx interface and frame start indication of Audio TDM Tx interface
A15	GPIO27	0	GPIO	3.3		
		1	SDIO_CLK	SDIO: 1.8/3.0; eMMC: 1.8	O	SDIO CLK
		2	RGMII_TXC	1.5(2.0)/2.5(1.0)	O	RGMII Tx clock
		3	AUDIO_TD1	3.0	O	Serial digital data output 1 of Audio Multi-channel I²S Tx interface and serial digital data of Audio TDM Tx interface
A16	GPIO28	0	GPIO	3.3		
		1	SDIO_CMD	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO CMD
		2	RGMII_TXD(0)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 0
		3	AUDIO_TD2	3.0	O	Serial digital data output 2 of Audio Multi-channel I²S Tx interface
B14	GPIO29	0	GPIO	3.3		
		1	SDIO_DAT(4)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 4
		2	RGMII_TXD(1)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 1
		3	AUDIO_TD3	3.0	O	Serial digital data output 3 of Audio Multi-channel I²S Tx interface

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
A17	GPIO30	0	GPIO	3.3		
		1	SDIO_DAT(5)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 5
		2	RGMII_TXD(2)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 2
		3	AUDIO_PWM0	3.0	O	Audio Pulse Width Modulation interface 0
B15	GPIO31	0	GPIO	3.3		
		1	SDIO_DAT(6)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 6
		2	RGMII_TXD(3)	1.5(2.0)/2.5(1.0)	O	RGMII Tx Data 3
		3	AUDIO_PWM1	3.0	O	Audio Pulse Width Modulation interface 1
A18	GPIO32	0	GPIO	3.3		
		1	SDIO_DAT(7)	SDIO: 1.8/3.0; eMMC: 1.8	I/O	SDIO Data input 7
		2	RGMII_RXC	1.5(2.0)/2.5(1.0)	I	RGMII Rx clock
		3	AUDIO_PWM2	3.0	O	Audio Pulse Width Modulation interface 2
B17	GPIO33	0	GPIO	3.3		
		1	RGMII_TX_CTL	1.5(2.0)/2.5(1.0)	O	RGMII Tx control
		2	AUDIO_PWM3	3.3	O	Audio Pulse Width Modulation interface 3
A19	GPIO34	0	GPIO	3.3		
		1	BLSP_I2C1_SCK(1)		I/O, OD	I²C1 SCK
		2	AUDIO_SPDIFIN(0)	3.0	I	Audio SPDIF input
B18	GPIO35	0	GPIO	3.3		
		1	BLSP_I2C1_SDA(1)		I/O, OD	I²C1 SDA
		2	AUDIO_SPDIFOUT	3.0 (confirm standard I/O voltage)	O	Audio SPDIF output
A62	GPIO36	0	GPIO	3.3		
		1	RMII0_TXD(0)	3.3	O	RMII0 Tx data 0
		2	LED(2)			led_clk or led_dat or led_strobe
		3	LED(0)			led_clk or led_dat or led_strobe
B58	GPIO37	0	GPIO	3.3		
		1	RMII0_TXD(1)	3.3	O	RMII0 Tx data 1
		2	WIFI0_WCI_OUT		O	Wi-Fi 0 LTE Coex output
		3	WIFI1_WCI_OUT		O	Wi-Fi 1 LTE Coex output
		4	LED(1)			led_clk or led_dat or led_strobe
A64	GPIO38	0	GPIO	3.3		
		1	RMII0_TX_EN	3.3	O	RMII0 Tx enable
		2	LED(2)			led_clk or led_dat or led_strobe

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
B59	GPIO39	0	GPIO	3.3		
		1	RMII0_RX_ER	3.3	I/O	RMII Rx error when master mode; RMII Tx error when slave mode
		2	PCIE_CLK_REQ_N(0)		OD	PCIe clock request (only use input mode)
		3	LED(3)			led_clk or led_dat or led_strobe
A63	GPIO40	0	GPIO	3.3		
		1	RMII0_REFCLK	3.3	I/O	Input reference clock when Slave mode. Output clock when Master mode
		2	WIFI0_RFSILIENT_BB(0)		I	Wi-Fi 0 RF silent signal (RF_Kill)
		3	WIFI1_RFSILIENT_BB(0)		I	Wi-Fi 1 RF silent signal (RF_Kill)
		5	LED(4)			led_clk or led_dat or led_strobe
		6	#PCIE_WAKEUP_N#		OD	
A65	GPIO41	0	GPIO	3.3		
		1	RMII0_RXD(0)	3.3	I	RMII0 Rx data 0
		2	WIFI0_CAL_XPA_ACTIVE		O	Wi-Fi I0 XPA control signal used for test purposes
		3	WIFI1_CAL_XPA_ACTIVE		O	Wi-Fi I1 XPA control signal used for test purposes
B60	GPIO42	0	GPIO	3.3		
		1	RMII0_RXD(1)	3.3	I	RMII0 Rx data 1
		2	WIFI_WCI_IN(0)		I	Wi-Fi LTE Coex input
B68	GPIO43	0	GPIO	3.3		
		1	RMII0_DV	3.3	I	RMII0 Rx valid
		2	WIFI_WCI_IN(1)		I	Wi-Fi LTE Coex input
B62	GPIO44	0	GPIO	3.3		
		1	RMII1_REFCLK	3.3	I/O	Input reference clock when Slave mode. Output clock when Master mode
		2	BLSP_SPI1_SCK	1.8/3.3	O	SPI1 serial clock
		3	SMART_ANT4(0)		I/O	wifi_2g TXPCU_ANTENNA_INFO[0] (from MAC) wifi_2g serial clock for smart antenna (serial mode)
B61	GPIO45	0	GPIO	3.3		
		1	RMII1_RXD(0)	3.3	I	RMII1 Rx data 0
		2	BLSP_SPI1_SS0_N	1.8/3.3	O	SPI1 chip select 0
		4	SMART_ANT5(0)		I/O	wifi_2g TXPCU_ANTENNA_INFO[1] (from MAC) wifi_2g serial Data for smart antenna (serial mode)
		5	LED(6)			led_clk or led_dat or led_strobe

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
B74	GPIO46	0	GPIO	3.3		
		1	RMII1_RXD(1)	3.3	I	RMII1 Rx data 1
		2	BLSP_SPI1_MOSI	1.8/3.3	O	SPI1 Master-out Slave-in data
		3	SMART_ANT6(0)		I/O	wifi_5g TXPCU_ANTENNA_INFO[0] (from MAC) wifi_5g serial clock for smart antenna (serial mode)
		4	LED(7)			led_clk or led_dat or led_strobe
A74	GPIO47	0	GPIO	3.3		
		1	RMII1_DV	3.3	I	RMII1 Rx valid
		2	BLSP_SPI1_MISO	1.8/3.3	I	SPI1 Master-in Slave-out data
		3	SMART_ANT7(0)		I/O	wifi_5g TXPCU_ANTENNA_INFO[1] (from MAC) wifi_5g serial Data for smart antenna (serial mode)
		4	LED(8)			led_clk or led_dat or led_strobe
B69	GPIO48	0	GPIO	3.3		
		1	RMII1_TX_EN	3.3	O	RMII Tx enable
		2	AUD_PIN_PCM_DTX	3.3	O	Transmitted data of Audio PCM interface
		4	LED(9)			led_clk or led_dat or led_strobe
A71	GPIO49	0	GPIO	3.3		
		1	RMII1_RX_ER	3.3	I/O	RMII Rx error when master mode; RMII Tx error when slave mode
		2	AUD_PIN_PCM_DRX		I	Received data of Audio PCM interface
			LED(10)			led_clk or led_dat or led_strobe
B72	GPIO50	0	GPIO	3.3		
		1	RMII1_TXD(0)	3.3	O	RMII1 Tx data 0
		2	AUD_PIN_PCM_PCLK		O	Clock of Audio PCM interface
		3	WIFI0_RFSILIENT_BB(1)		I	Wi-Fi 0 RF silent signal (RF_Kill)
		4	WIFI1_RFSILIENT_BB(1)		I	Wi-Fi 1 RF silent signal (RF_Kill)
		5	LED(11)			led_clk or led_dat or led_strobe
		6	#PCIE_WAKEUP_N#		OD	
B73	GPIO51	0	GPIO	3.3		
		1	RMII1_TXD(1)	3.3	O	RMII1 Tx data 1
		2	AUD_PIN_PCM_FSYNC			Frame start indication of Audio PCM interface
		3	WIFI0_CAL_XPA_ACTIVE			Wi-Fi 0 XPA control signal used for test purposes
		4	WIFI1_CAL_XPA_ACTIVE			Wi-Fi 1 XPA control signal used for test purposes

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
A77	GPIO52	0	QPIC_PAD_TE	3.3	OD	LCD control info, V sync
		2	MDC	3.3	O	Management Data Clock
		3	PCIE_CLK_REQ_N(1)	3.3		PCIe clock request (only use input mode)
		4	AUDIO_TXMCLK(1)	3.0	I/O	Master clock source of Audio I²S/ TDM Tx interface
			BOOT_CONFIG(13)			
A66	GPIO53	0	GPIO	3.3		
		1	QPIC_PAD_BUSY_N		I, OD	NAND controller busy_not_ready input. Active low.
		2	MDIO	3.3	I/O, OD	Management Data I/O
		3	AUDIO_TXBCLK(1)	3.3		Serial digital data output 1 of Audio Multi-channel I²S Tx interface and serial digital data of Audio TDM Tx interface
A79	GPIO54	0		I/O	I/O	
		1	QPIC_PAD_LCD_ RS_N		O	LCD controller RESX, reset signal. Active low
		2	BLSP_SPI0_SS0_N(1)	3.3	O	SPI0 chip select 0
		3	AUDIO_TD1	3.3	O	Serial digital data output 1 of Audio Multi-channel I²S Tx interface and serial digital data of Audio TDM Tx interface
A67	GPIO55	0	GPIO	3.3		
		1	QPIC_PAD_WE_N		O	NAND/LCD controller write enable
		2	BLSP_SPI0_MOSI(1)	3.3	O	SPI0 Master-out Slave-in data
		3	AUDIO_TD2	3.3	O	Serial digital data output 2 of Audio Multi-channel I²S Tx interface and serial digital data of Audio TDM Tx interface
			BOOT_CONFIG(9)	3.3	I	
B63	GPIO56	0	GPIO	3.3		
		1	QPIC_PAD_OE_N		O	NAND/LCD controller read enable
		2	BLSP_SPI0_SCK(1)		O	SPI0 serial clock
		3	AUDIO_TD3	3.3	O	Serial digital data output 3 of Audio Multi-channel I²S Tx interface
			BOOT_CONFIG(10)	3.3	I	
A69	GPIO57	0	GPIO	3.3		
		1	QPIC_PAD_DAT(3)		O	NAND/LCD controller data
		2	BLSP_SPI0_MISO(1)		I	SPI0 Master-in Slave-out data
		3	AUDIO_TXFSYNC(1)	3.3	I/O	Left or Right indication of Audio I2S Tx interface and frame start indication of Audio TDM Tx interface

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
B66	GPIO58	0	GPIO	3.3		
		1	QPIC_PAD_DAT(5)		O	NAND/LCD controller data
		2	LED[2]	3.3	O	
		3	BLSP_I2C0_SCK(2)	3.3	IO, OD	I2C serial clock
		-				
		5	SMART_ANT6	3.3	IO	Smart antenna
		6	AUDIO_RXMCLK(1)	3.3	I/O	Master clock source of Audio I2S/ TDM Rx interface
A72	GPIO59	0	GPIO	3.3		
		1	QPIC_PAD_DAT(6)		O	NAND/LCD controller data
		2	BLSP_I2C0_SDA(2)	3.3	IO, OD	I2C serial data
		-				
		4	SMART_ANT7	3.3	IO	Smart antenna
		5	AUDIO_SPDIFIN(1)	3.3	O	Audio SPDIF input
B65	GPIO60	0	GPIO	3.3		
		1	QPIC_PAD_DAT(7)		O	NAND/LCD controller data
		2	BLSP_UART0_RXD(1)	3.3	I	UART receive data
		-				
		4	SMART_ANT4	3.3	IO	Smart antenna
		5	LED[0]	3.3	O	
		6	AUDIO_TXBCLK	3.3	IO	Audio transmit bit clock
		7	AUDIO_RXBCLK	3.3	IO	Audio receive bit clock
A78	GPIO61	0	GPIO	3.3		
		1	QPIC_PAD_LCD_ CS_N		O	LCD controller chip select
		2	BLSP_UART0_TXD	3.3	O	UART transmit data
		3	SMART_ANT5(1)	3.3	I/O	Smart antenna
		4	SMART_ANT3(3)	3.3	I/O	Smart antenna
		5	LED(1)	3.3	O	
		6	AUDIO_TXFSYNC(2)	3.3	I/O	Audio transmit frame sync
		7	AUDIO_RXFSYNC(2)	3.3	I/O	Audio receiver frame sync
A70	GPIO62	0	GPIO	3.3		
		1	QPIC_PAD_CLE_ LB_N		O	NAND controller CLE/LCD controller DCX. CLE is command latch enable. Active high. DCX is data/command. 1 is data, 0 is command.
		2	CHIP_RST_OUT	3.3	O	Chip reset signal
		3	WIFI0_UART_TXD	3.3	O	Wi-Fi 0 UART transmit data
		4	WIFI1_UART_TXD	3.3	O	Wi-Fi 1 UART transmit data
		5	AUDIO_SPDIFOUT	3.3	O	Audio SPDIF output
			BOOT_CONFIG(11)	3.3	I	

Pin ID	Pin name	GPIO CFG. FUNC_SEL	Configurable Function	Voltage	Type	Description
A68	GPIO63	0	GPIO	3.3		
		1	QPIC_PAD_NAND_CS_N		O	NAND controller chip select
		2	WIFI0_UART_RXD	3.3	I	Wi-Fi 0 UART receive data
		3	WIFI1_UART_RXD	3.3	I	Wi-Fi 1 UART receive data
		4	WIFI1_UART_TXD	3.3	I	Wi-Fi 1 UART transmit data
		5	AUDIO_TXD[1]	3.3	O	Audio transmit data
		6	AUDIO_RXD	3.3	I	Audio receive data
		7	AUDIO_SPDIFOUT	3.3	O	Audio SPDIF out
		8	AUDIO_SPDIFIN	3.3	I	Audio SPDIF in
A73	GPIO64	0	GPIO	3.3	IO	
		1	QPIC_PAD_DAT(1)		O	NAND/LCD controller data
		2	AUDIO_PWM0	3.3		Audio Pulse Width Modulation interface 0
A76	GPIO65	0	GPIO	3.3		
		1	QPIC_PAD_DAT(2)		O	NAND/LCD controller data
		2	AUDIO_PWM1	3.3		Audio Pulse Width Modulation interface 1
B71	GPIO66	0	GPIO	3.3		
		1	QPIC_PAD_DAT(3)		O	NAND/LCD controller data
		2	AUDIO_PWM2	3.3		Audio Pulse Width Modulation interface 2
B67	GPIO67	0	GPIO	3.3		
		1	QPIC_PAD_DAT(0)		O	NAND/LCD controller data
		2	AUDIO_PWM3	3.3		Audio Pulse Width Modulation interface 3
B64	GPIO69	0	GPIO	3.3		
		1	QPIC_PAD_ALE_LB_N		O	NAND controller ALE. Active high.

TABLE 3-10. PIN STATUS ON BOOT

Pin ID	Pin name	Signal name	Bootstrap value description	Bootstrap default value
A81	GPIO3	Apps_auth_enable	Authentication enable 0: no auth 1: auth required	0
A10	GPIO14	boot_interface [0]	Boot_interface[1:0]=00: use spi as boot Boot_interface[1:0]=01: use emmc as boot Boot_interface[1:0]=10: use qpic as boot Boot_interface[1:0]=00: boot from usb	00
B73	GPIO51	Boot_interface [1]		
NC*	GPIO15	Watchdog_enable	Watchdog_enable 0: watchdog disable 1: watchdog enable	1
B17	GPIO33	All_use_serial_num_inv	Use serial num for secure boot authentication 0: Use serial num 1: Use OEM ID (default)	1
A62	GPIO36	Boot_from_rom	0: boot from code RAM 1: boot from ROM	0
B58	GPIO37	Apps pbl boot speed [0]	APPS PBL BOOT SPEED (APSS PLL) 00 – XO clock 48MHz 01 – FE_PLL clock – 200MHz 10 – FE_PLL clock – 500MHz 11 – Reserved	00
A64	GPIO38	Apps pbl boot speed [1]		
A67	GPIO55	Force_usb_boot	0: not force boot from USB 1: force boot from USB	0
B63	GPIO56	pi_mode	0: Function mode	0
A70	GPIO62	Jtag_boot_en	0: GPIO0-GPIO5 are normal GPIO 1: GPIO0-GPIO5 are used as JTAG interface	0
B64	GPIO69	Pk_hash_index_src	Select ROM PK hash index source 0: from QC ffuse 1: From OEM efuse	0

4. Electrical characteristics

TABLE 4-1. POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units
DVDD33	3.3V Supply Voltage	3.0	3.3	3.6	V

TABLE 4-2. TEMPERATURE LIMIT RATINGS

Parameter	Minimum	Maximum	Units
Storage Temperature (Commercial)	-40	+70	°C
Storage Temperature (Industrial)	-40	+90	°C
Commercial Operating Temperature	0	+65	°C
Industrial Operating Temperature	-40	+85	°C
Humidity	10	90	%RH
Storage humidity	5	90	%RH

5. Power management

5.1. Power consumption

TABLE 5-1. POWER CONSUMPTION

DBS			Voltage	Current	Total power in Watts
Tx	2x2	MCS0	12	0.96	11.5
		MCS9	12	0.8	9.6
Rx	2x2	MCS0	12	0.55	6.6
		MCS9	12	0.64	7.6

NOTE: Power consumption was measured while generating throughput via WiFi and all Ethernet ports using DVK

6. Radio characteristics

2.4GHZ 802.11G 20MHZ

	6 Mbps	9 Mbps	12 Mbps	18 Mbps	24 Mbps	36 Mbps	48 Mbps	54 Mbps	-	-
Transmitter Power (dBm)	22	22	21	21	21	20	19	18	-	-
Receiver sensitivity (dBm)	-94	-93	-92	-90	-87	-86	-81	-79	-	-

2.4GHZ 802.11N/AC 20MHZ

	MCS 0	MCS 1	MCS 2	MCS 3	MCS 4	MCS 5	MCS 6	MCS 7	MCS 8	-
Transmitter Power (dBm)	22	21	21	20	18	17	15	14	13	-
Receiver sensitivity (dBm)	-93	-90	-88	-85	-80	-76	-74	-72	-68	-

2.4GHZ 802.11N/AC 40MHZ

	MCS 0	MCS 1	MCS 2	MCS 3	MCS 4	MCS 5	MCS 6	MCS 7	MCS 8	MCS 9
Transmitter Power (dBm)	22	21	21	20	18	17	15	14	13	12
Receiver sensitivity (dBm)	-90	-88	-85	-82	-77	-73	-73	-70	-66	-64

5GHZ 802.11N/AC 20MHZ

	MCS 0	MCS 1	MCS 2	MCS 3	MCS 4	MCS 5	MCS 6	MCS 7	MCS 8	-
Transmitter Power (dBm)	21	21	20	19	18	17	16	16	15	-
Receiver sensitivity (dBm)	-92	-89	-86	-83	-80	-76	-74	-73	-68	-

5GHZ 802.11N/AC 40MHZ

	MCS 0	MCS 1	MCS 2	MCS 3	MCS 4	MCS 5	MCS 6	MCS 7	MCS 8	MCS 9
Transmitter Power (dBm)	21	21	20	19	18	17	16	16	15	14
Receiver sensitivity (dBm)	-89	-86	-84	-81	-78	-73	-72	-70	-68	-67

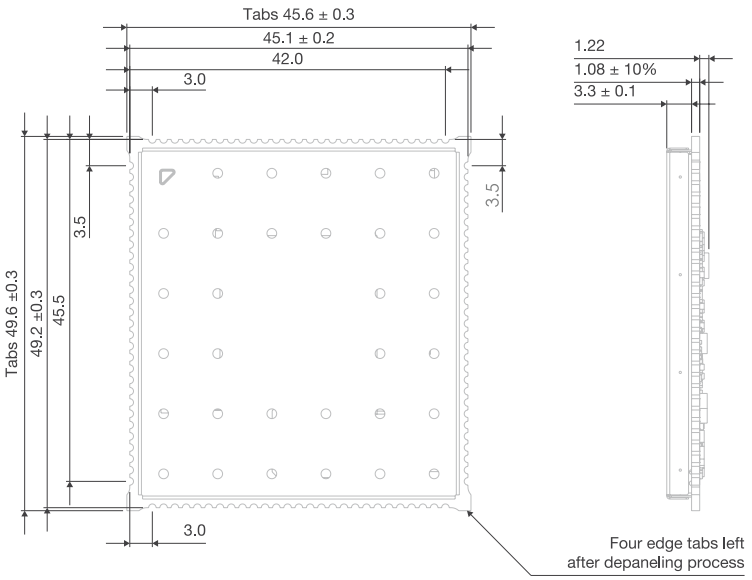
5GHZ 802.11AC 80MHZ

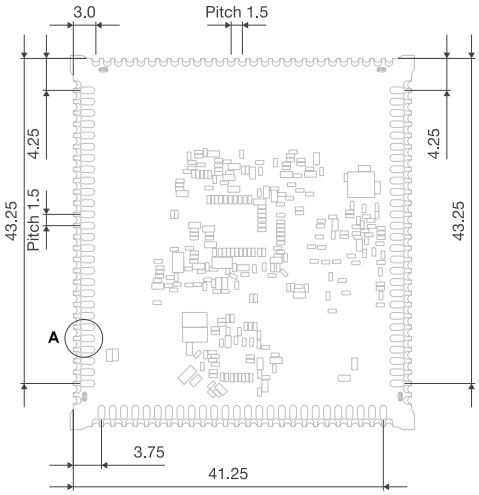
5GHz 802.11ac VHT80	MCS 0	MCS 1	MCS 2	MCS 3	MCS 4	MCS 5	MCS 6	MCS 7	MCS 8	MCS 9
Transmitter Power (dBm)	21	20	19	19	18	17	16	16	15	14
Receiver sensitivity (dBm)	-86	-83	-80	-77	-74	-70	-69	-67	-63	-61

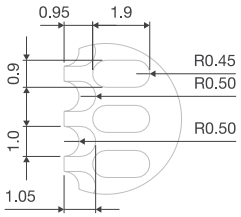
Note:

1. Receiver sensitivity and Transmitter Power tolerance is +-2dB
2. In the table above output power is specified per chain, each radio 2.4GHz and 5GHz has two chain each, because total power is double or 3dB higher.

7. Mechanical characteristics

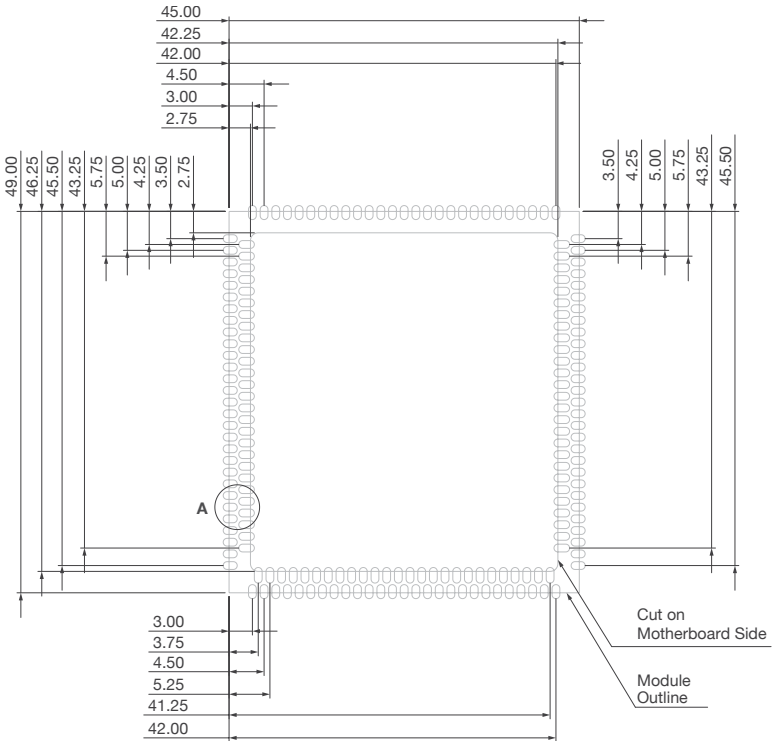


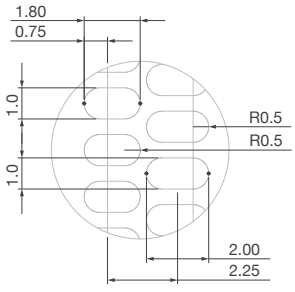




DETAIL A
SCALE 8 : 1

PCB footprint





DETAIL A
SCALE 8 : 1

8. Design considerations

8.1. Ethernet interface

ETHERNET DESIGN GUIDELINES:

Category	Guidelines/Remarks
Groups	P[0..4]_TRX[0..3]+, P[0..4]_TRX[0..3]-
Route type	Differential pair, 100 Ohm impedance
Length	< 1.5 in., try to route as short as possible
Length match within pair	+-5 mils
Length match across pairs	There is no requirement to length match the Tx and Rx pairs
Spacing requirements	3 W spacing between pairs and to other signals
Vias/layer transitions	Minimize layer transitions; where necessary limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of signal vias
Other	Each pair needs magnetic module (or combo module for all pairs) between PHY and Ethernet port

8.2. USB

USB 3.0 DESIGN GUIDELINES:

Category	Guidelines/Remarks
Groups	USB_TXP, USB_TXN
Route type	Differential pair, 100 Ohm impedance for the super speed pairs according to USB3.0 specification
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	+- 5 mils
Length match across pairs	There is no requirement to length match the Tx and Rx pairs
Spacing requirements	3 W spacing between pairs and to other signals
Vias/layer transitions	Avoid layer transitions and vias
AC coupling	Use 0.1 uF capacitors on each signal line of the Tx pair from Habanero module; place them symmetrically at the same point on the pair
Other	Clear the GND pour under the signal pads of the connector where SMD connectors are used

USB 2.0 DESIGN GUIDELINES:

Category	Guidelines/Remarks
Groups	(USB2_DP, USB2_DM) and (USB1_DP, USB1_DM)
Route type	Differential pair, 90 Ohm impedance for the USB2.0 pair according to USB2.0 specification
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	+- 5 mils
Length match across pairs	Not applicable
Spacing requirements	3 W spacing between pairs and to other signals
Vias/layer transitions	Avoid layer transitions and vias
AC coupling	Not applicable; the lines must be DC connected
Other	Clear the GND pour under the signal pads of the connector where SMD connectors are used

8.3. Parallel NAND flash / LCD

NAND FLASH DESIGN GUIDELINES:

Category	Guidelines/Remarks
Signal/group	QPIC_PAD_NAND_CS_N QPIC_PAD_CLE_LB_N QPIC_PAD_ALE_LB_N QPIC_PAD_WE_N QPIC_PAD_OE_N QPIC_PAD_BUSY_N QPIC_PAD_DATA[7:0]
Route type	Single-ended
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match	200 mils within group, 400 mils across groups
Spacing requirements	2 W spacing to other signals
GND shielding	Not required
Vias/layer transitions	Vias are acceptable
Voltage	3.3 V
Decoupling and power layout	Follow best design practices and provide decoupling close to the NAND device. • Allocate one 0201 decap per pin and locate close to the pin • A bulk capacitor in the order of 1 uF or more is advised for the device • Share the 3.3 V power plane
Other	Some NAND controller output lines are used at power-up to sense boot configuration straps. Take care to minimize stubs in the path. A 10K pull-up is recommended on the NAND_CS signal at flash device

LCD DESIGN GUIDELINES:

Category	Guidelines/Remarks
Signal/group	QPIC_PAD_LCD_CS_N QPIC_PAD_CLE_LB_N QPIC_PAD_LCD_RS_N QPIC_PAD_ALE_LB_N QPIC_PAD_WE_N QPIC_PAD_OE_N QPIC_PAD_BUSY_N QPIC_PAD_DATA[8:0]
Route type	Single-ended 50 Ohm impedance
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Spacing requirements	2 W spacing to other signals
GND shielding	Not required
Vias/layer transitions	Vias are acceptable
Voltage	3.3 V
Voltage	3.3 V
Decoupling and power layout	Follow best design practices and provide decoupling close to the NAND device. • Allocate one 0201 decap per pin and locate close to the pin • A bulk capacitor in the order of 1 uF or more is advised for the device Share the 3.3 V power plane

8.4. I2C

I2C DESIGN GUIDELINES:

Category	Guidelines/Remarks
Signal/group	I2C_SDA, I2C_SCL
Spacing	As open drain signaling is used by the interface, these signals are susceptible to crosstalk from strongly driven aggressors. A spacing of 2 W is recommended at the minimum from other signals
Loading	Run the traces short to the devices and reduce capacitive load
Voltage	The IPQ4029 chip operates this interface at 3.3 V and the input will not withstand higher voltage. Level converters are recommended to work with I2C devices at higher voltage

8.5. SD/eMMC

SDIO DESIGN GUIDELINES:

Category	Guidelines/Remarks	
Signal/group	**Configurable function**	**Pin name**
	SDIO_CD	GPIO22
	SDIO_CLK	GPIO27
	SDIO_DAT[0]	GPIO23
	SDIO_DAT[1]	GPIO24
	SDIO_DAT[2]	GPIO25
	SDIO_DAT[3]	GPIO26
	SDIO_DAT[4]	GPIO29
	SDIO_DAT[5]	GPIO30
	SDIO_DAT[6]	GPIO31
	SDIO_DAT[7]	GPIO32
Route type	Single-ended 50 Ohm impedance	
Return path	Ensure continuous and unbroken return path without voids	
Length	< 4.5 in.	
Length match	10 mils within group	
Spacing requirements	2 W spacing to other signals	
GND shielding	Now required	
Vias/layer transitions	Vias are acceptable	
Voltage	1.8 V / 3.3 V auto change according to SD card If configured as eMMC interface, it is fixed 1.8 V	
Decoupling and power layout	Follow best design practices and provide decoupling close to the SDIO device. • Allocate one 0201 decap per pin and locate it close to the pin • A bulk capacitor in the order of 1 MF or more is advised for the device	
Other	Pay attention to SDIO_CLK, add 22 Ohm damping resistor and 5 pF paralleled cap to GND	

8.6. PCIe

PCIE DESIGN GUIDELINES FOR DATA SIGNALS:

Category	Guidelines/Remarks
Signal/group/group	PCIE_TXP, PCIE_TXN PCIE_RXP, PCIE_RXN
Route type	Differential pair 100 Ohm impedance
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	+- 5mils
Length match across pairs	There is no requirement to length match the Tx and Rx pairs
Spacing requirements	3 W spacing between pairs and other signals after the breakout from module
GND shielding	Provide GND shield at 3 W spacing away from the signal pairs. The GND shape must be stitched to the main GND in inner layers with vias at regular intervals of 100 mils
Vias/layer transitions	Avoid layer transitions
AC coupling	There are already 0.1 uF capacitors on each signal line of the Tx pair on the module; No additional coupling is needed
Voltage	The voltage rails for the PCIe interface are implemented with filters for the PLL (AVDDPLL_PCIE) and the I/O (AVDD) rails
Other	Clear the GND pour under the paired signal pads of the connector where SMD connectors are used

PCIE DESIGN GUIDELINES FOR REFCLK:

Category	Guidelines/Remarks
Signal/group	PCIE_CLKOUTN, PCIE_CLKOUTTP
Route type	Differential pair 100 Ohm impedance
Return path	Ensure continuous and unbroken return path without voids
Length	< 5 in.
Length match within pair	+- 5 mils
Length match across pairs	There is no specific requirements to match lengths across different REFCLK pairs
Spacing requirements	3 W spacing between pairs and to other signals after the breakout from the module
GND shielding	Provide GND shield at 3 W spacing away from the signal pairs. The GND shape must be stitched to the main GND in inner layers with vias at regular intervals of 100 mils
Vias/layer transitions	Minimize layer transitions. Where necessary, limit to 2 vias per signal trace. Provide return vias interconnecting the GNDs in the immediate vicinity of the signal vias. These vias should form a symmetric GSSG pattern and recommend clearing an oblong void at this transition point through layers
AC coupling	Should not be used. The REFCLK must be DC connected to the loads

8.7. JTAG

JTAG DEBUG INTERFACE DESIGN GUIDELINES:

Category	Guidelines/Remarks
Signal/group	JTAG_TRST_N, JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TCK, JTAG_RST_N(SRST)
Mechanical	Ensure sufficient clearance for placement of debug headers
Spacing	2 W spacing is desirable
Routing	Route short (< 5 in.) and direct traces with impedance control
Length match	No critical requirement; recommend keeping the signals matched within 500 mils
Voltage	Operates at 3.3 V; the PowerTrace debugger can be connected directly

9. Thermal considerations

Recommended heatsink area for a reference power dissipation is should be at least 180 square centimeters. Maximum ambient temperature with the given heatsink is +85ºC.

Thermal flow equals GND current flow

- Heat flows where current flows – in copper
- Greater copper cross section
  - More heat flow, more current flow through Via and GND structure

Vertical copper cross section

- Move the heat to other layers
- Internal layers conduct heat horizontally

Horizontal copper cross section

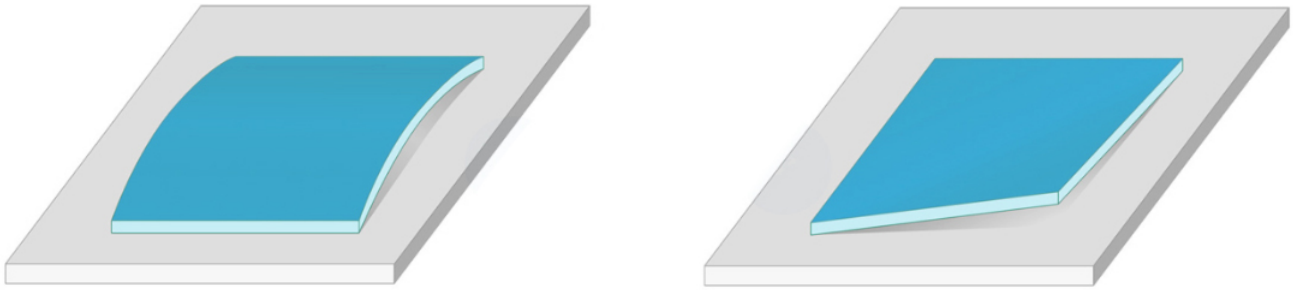
- Avoid fence of non-GND vias (reduce horizontal copper)
- Internal layers cannot get rid of heat
- Heat can be trapped on inner layers
- Opening the solder mask in top and bottom layers beneath the heat parts is the better way of radiating heat
- Also to have maximum GND copper possible with vertical copper (vias) to move heat from inner layers

10. Laminate Conditions

10.1. Bow and Twist

8devices modules are manufactured according to the standard IPC-A-610 Norm Class 2.
Standard states: “Bow/twist after solder should not exceed 1.5% for through-hole and 0.75% for surface mount printed board applications”.
According to this statement, Habanero module can be bowed and twisted up to 0.367mm.
To avoid negative effects of bow and twist we recommend to increase the paste thickness for the module pads to achieve better co-planarity.

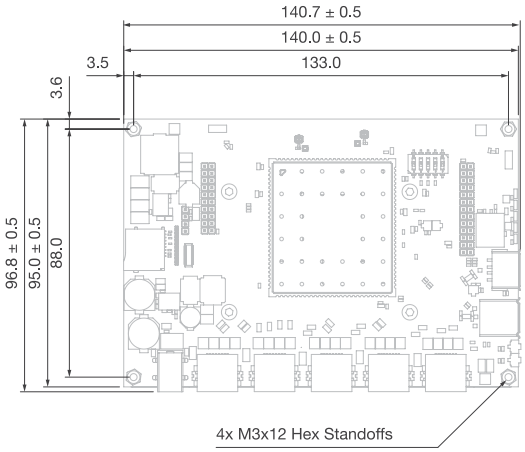
FIGURE 10-1. EXAMPLE OF BOW AND TWIST

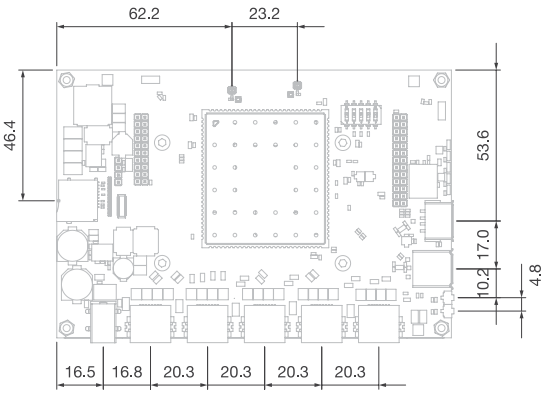


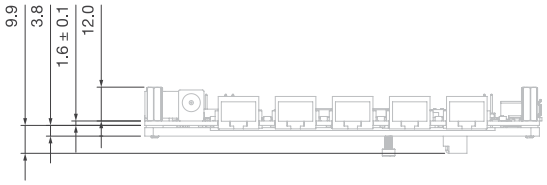
Bow **Twist**

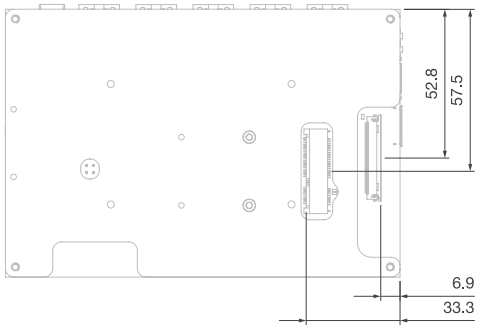
11. Development board

11.1. DVK dimensions with heatsink

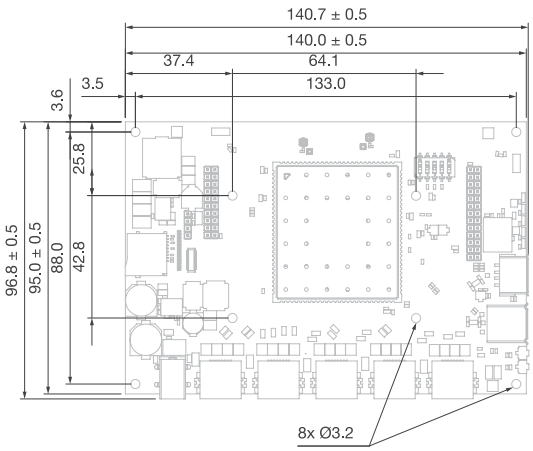


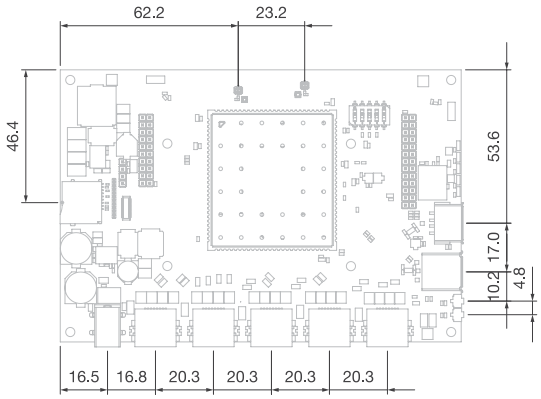


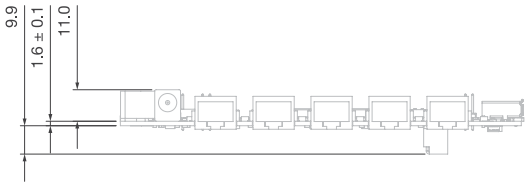


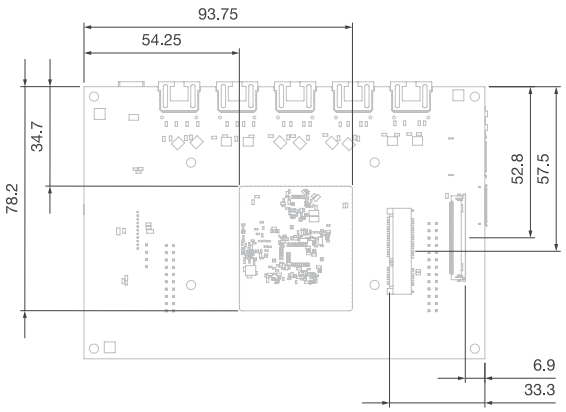


11.2. DVK dimensions without heatsink

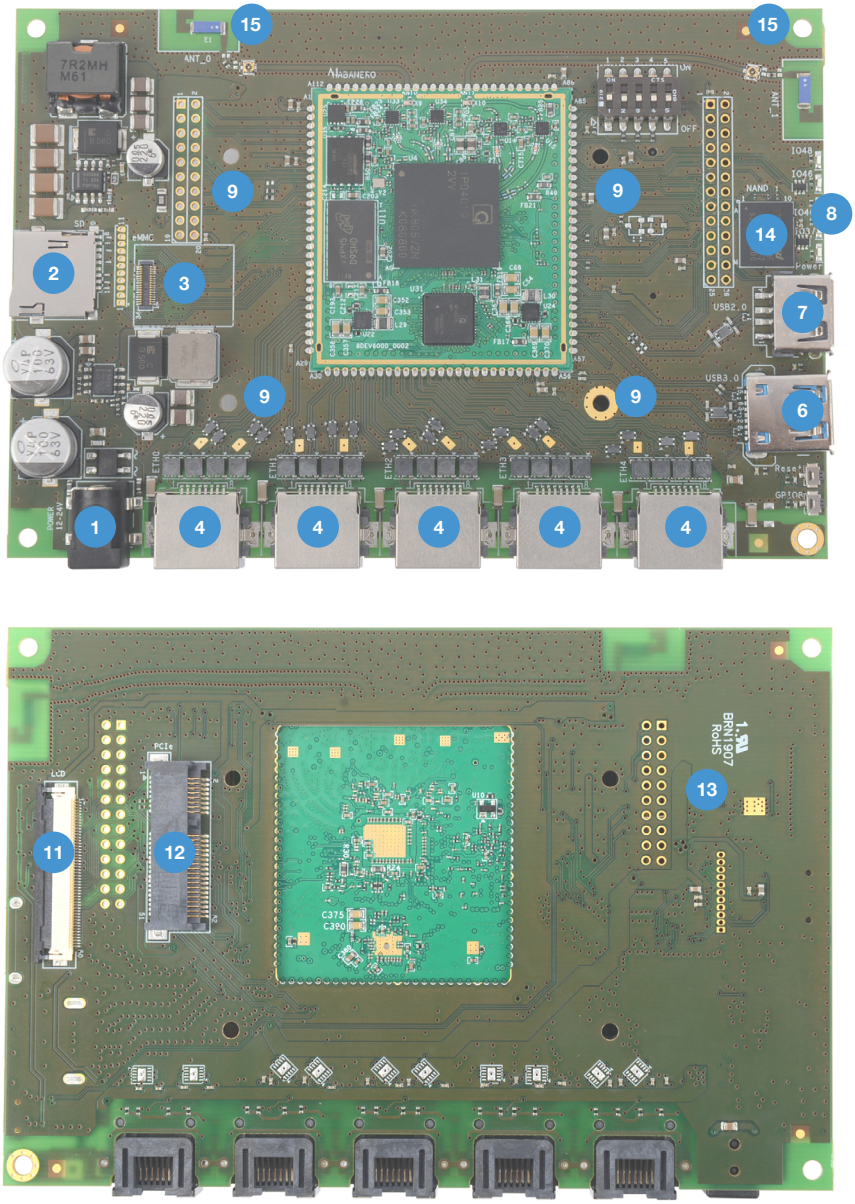






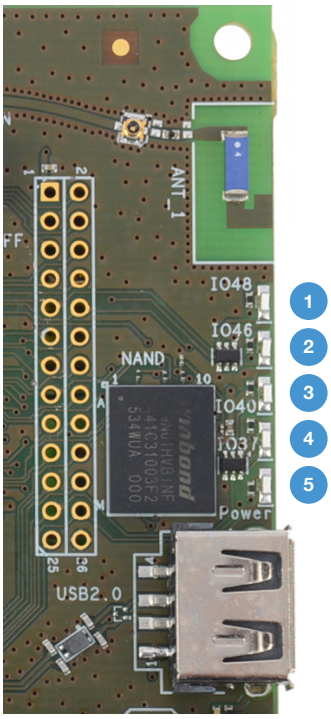


11.3 DVK interfaces



1. Power 12V-24V
2. SD card socket
3. eMMC connector
4. Ethernet port
5. Buttons (Reset, GPIO8)
6. USB 3.0 (5V 1A)
7. USB 2.0 (5V 1A)
8. LEDs
9. Heatsink screws
10. Habanero module
11. FPC connector
12. PCIe connector
13. Heatsink
14. External NAND place
15. Dual-band antennas

11.4 LEDs



LED number	Description
1	GPIO48
2	GPIO46
3	GPIO40
4	GPIO37
5	Power

11.5 BOOTSTRAP switch

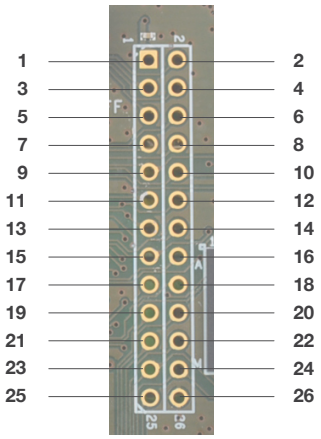
	1	2	3	4	5
	JTAG_EN	USB_BOOT	GPIO14	GPIO51	Not connected
ON	GPIO0~GPIO5 are used as JTAG interface.	Force boot from USB	1	1	-
OFF	GPIO0~GPIO5 are normal GPIOs.	Normal boot	0	0	-

GPIO14 AND GPIO51 CONFIGURATION

GPIO51	GPIO14	Function description
0	0	Boot interface is SPI
0	1	Boot interface is eMMC
1	0	Boot interface is QPIC
1	1	Boot from USB

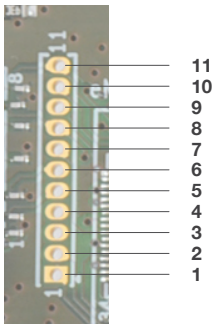
11.6 DVK header pinout

J13



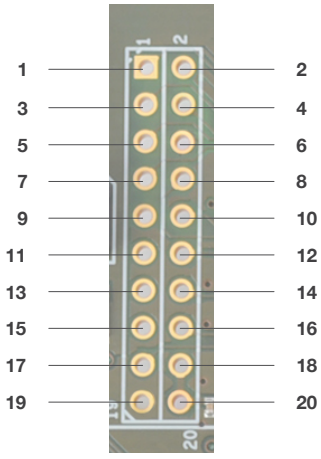
Header pin	GPIO	Header pin	GPIO	Header pin	GPIO
1	3,3	10	GPIO61	19	GPIO45
2	GPIO2	11	GPIO51	20	GPIO41
3	GPIO0	12	GPIO52	21	GPIO42
4	GPIO1	13	GPIO50	22	GPIO39
5	GPIO4	14	GPIO47	23	GPIO40
6	GPIO3	15	GPIO48	24	GPIO37
7	GPIO5	16	GPIO49	25	GPIO36
8	GPIO54	17	GPIO43	26	GND
9	GPIO46	18	GPIO44	-	

J17



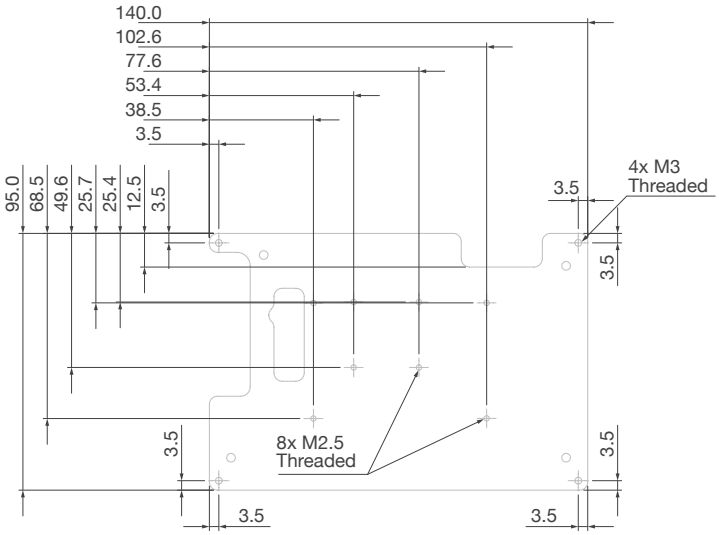
Header pin	GPIO	Header pin	GPIO
1	GPIO30	7	GPIO25
2	GPIO29	8	GPIO24
3	GPIO23	9	GPIO32
4	GPIO27	10	GPIO31
5	GPIO26	11	GPIO22
6	GPIO28	-	-

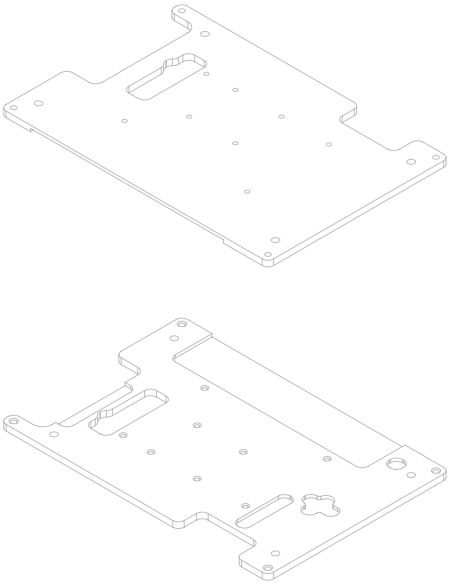
J18



Header pin	GPIO	Header pin	GPIO	Header pin	GPIO
1	GPIO8	8	3.3V	15	CHIP_ RST_OUT
2	GND	9	GPIO18	16	GPIO34
3	GPIO11	10	GPIO20	17	5V
4	UART_ RXD	11	GPIO21	18	3.3V
5	GPIO10	12	GPIO33	19	GND
6	UART_ TXD	13	GND	20	3.3V
7	GPIO09	14	GPIO35	-	-
8	GPIO54	17	GPIO43	26	GND
9	GPIO46	18	GPIO44	-	

11.7 DVK heatsink





12. Habanero packaging and ordering info

Habanero modules are packed into trays. Each tray fits 15 modules.
Every 5 trays are vacuum sealed and one standard packaging box contains 375 modules.

FIGURE 12-1. HABANERO TRAY DIMENSIONS

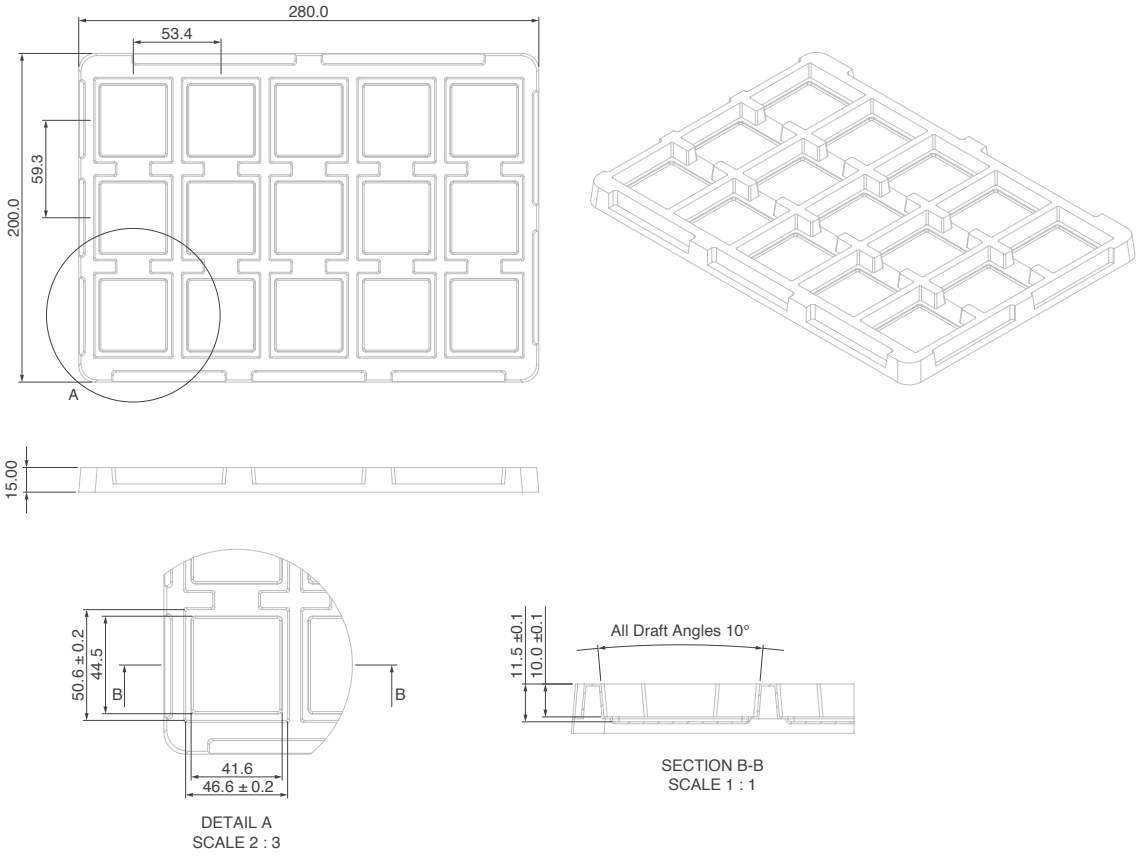


FIGURE 12-2. STANDARD PACKAGING BOX DIMENSIONS

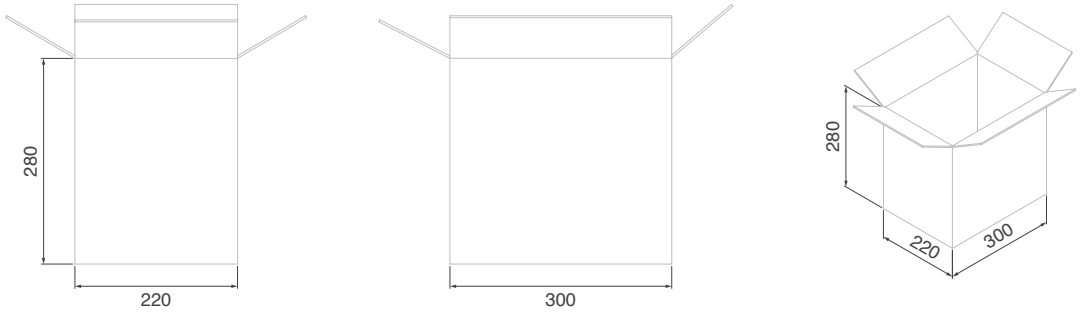


TABLE 12-3. ORDERING PART NUMBERS

Habanero	Habanero module, commercial temperature range 0°C to 65°C, IPQ 4019 SoC
Habanero-I	Habanero module, industrial temperature range -40°C to 85°C, IPQ 4029 SoC
Habanero-DVK	Development kit, based on Habanero module, IPQ 4019 SoC

13. Document Revision History

Revision	Revision Date	Description
v1.0	2019-08-05	Initial release.
v1.1	2019-08-14	Updated mechanical and added product packaging and ordering info.
v1.2	2019-09-06	Updated J18 header pin 6 description on page 28.
v1.3	2020-02-06	Updated table 3-2 (page 6) and table 3-9 (page 12). Pin ID B17 to B16.
v1.4	2022-12-21	Product drawings updated.
v1.5	2023-01-10	Laminate conditions chapter added
v1.6	2023-05-29	Product specification updated